Nanofabrication down to 10 nm on a plastic substrate

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Over past few decades, there has been increasing attention to high-frequency electronic devices on plastic or flexible substrate[1, 2] but with limited progress so far. One of the roadblocks is the difficulty in realizing sub-100 nm fabrication on a plastic substrate to afford multi-GHz transistors. Although sub-10 nm fabrication had been routinely achieved via e-beam lithography (EBL) or step-flash imprint lithography (S-FIL) on silicon substrates, applying them onto plastic substrates is not straightforward. Here, we report our investigation on enabling 10 nm EBL and high-throughput S-FIL on a polyimide substrate.

Polyimide sheets (25~100 μm thick) were selected as the substrate because of its high glass transition temperature and mechanical strength. Liquid polyimide surface coating followed by thermal curing was employed to significantly improve the interface smoothness as shown in Table 1. This step is critical for the best resolution from EBL and S-FIL. Another critical detail in this work is to assure the pattern fidelity by using a charge compensating conductive polymer (Espacer®) in direct contact with the e-beam ground plane. EBL was performed at 30 keV with beam current ~28 pA using Raith® system on a ZEISS® SEM. Grooves with 10 ±1.4 nm in width were obtained in 55 nm thick PMMA on thin polyimide loaded on silicon as shown in Figure 1a. Figure 1b demonstrated successful lift-off of 25 nm wide Ti gratings after EBL on a thick stand-alone polyimide substrate. The high resolution EBL and lift-off results are benefits from the cold development at 4 ^{o}C in IPA : MIBK (3:1) with 1.5 vol % methyl ethyl ketone (MEK) as first reported on silicon substrate.[3] It requires almost double dose for the development at 4 ^{o}C compared to room temperature as depicted by contrast curves in Figure 2. Compared to 70 nm fine features reported on plastic substrates,[4,5] this is the first report of 10 nm EBL and 25 nm lift-off gratings on polyimide substrates as far as we are aware of. Based on our preliminary results, dual-finger gated graphene field-effect transistors (GFET), figure 3, with short-channel below 50 nm on a plastic substrate will be demonstrated for the first time. Such devices are expected to enable aforementioned high-speed GHz applications. As a possible route for high-throughput fabrication of these flexible GFETs, S-FIL was investigated and sub-100 nm gratings (resolution limited to the available template) on 2'' round polyimide substrate was demonstrated in Figure 4. S-FIL of sub-50 nm short channel for GFET on polyimide substrates is in the experiment.

In this work, we have shown the feasibility of nanofabrication down to 10 nm on a plastic substrate using conventional EBL. High throughput S-FIL with high resolution (20-50 nm) will also be demonstrated on plastic substrates. This paves the way for fundamental studies and large-scale manufacturing of nanoelectronics with advanced performance on plastic substrates.

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3. *W. Hu, et al., J. Vac. Sci. Technol. B 22, 1711 (2004) **22** (4), 1711-1716 (2004).*
4. *Z. Z. Bandic, et al., Microsyst Technol **13** (8-10), 817-823 (2007).*
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Table 1. Comparison on the surface roughness of polyimide substrate before and after treatment

Polyimide substrate	Surface roughness (RMS) by AFM	
	Local (5×5 μm^2)	Global (50×50 μm^2)
As-received	~2 nm	≥200 nm
After 2-3 cycles of polymer coating	~ 0.3 nm	⩽10 nm
After 5-10 cycles of polymer coating	~ 0.3 nm	⩽3 nm

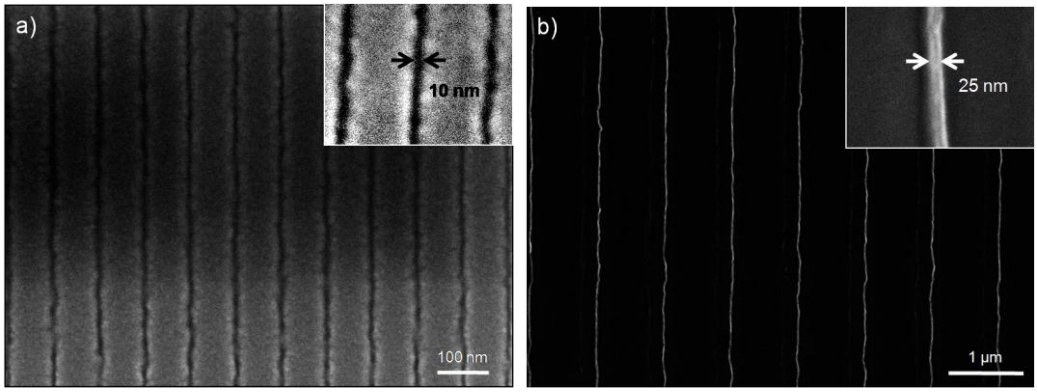

Figure 1: Sub 30 nm polymer and metal features fabricated on plastic surfaces: a) e-beam lithography (EBL) of sub-10 nm grooves in ~55 nm thick PMMA resist on thin polyimide coated on silicon wafer; b) 25 nm Ti gratings by lift-off after EBL on a thick standalone polyimide substrate. Both insets showed the measurements and all EBL was performed on a SEM Raith® system at 30 keV and developed at 4 °C.

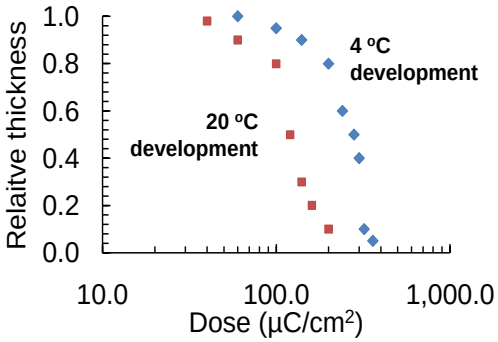

Figure 2: Development contrast curve of PMMA on polyimide substrate at 4 °C and 20 °C. Relative thickness denotes the ratio of residual thickness of exposed PMMA after the development to the original thickness. 1.0 and 0.0 indicate no and all PMMA has been developed, respectively.

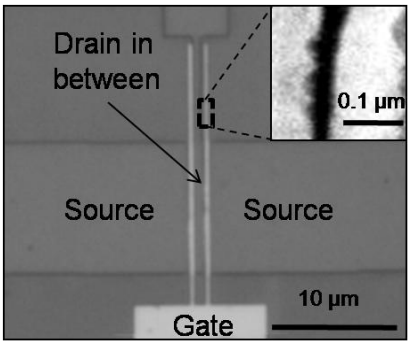

Figure 3: *The structure of dual-finger gated graphene field-effect transistors (GFET) on a polyimide substrate.* The device here has gate length ~200 nm, and sub-50 nm will be demonstrated in this work.

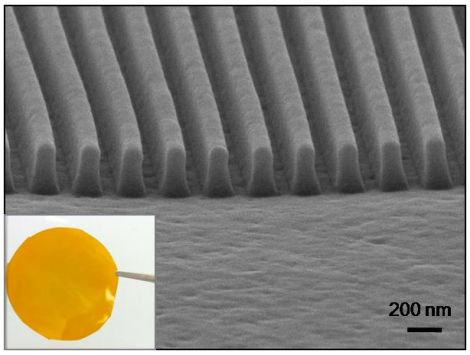

Figure 4: Step-flash imprint lithography of gratings with 100 nm half-pitch in ~240 nm height on 2'' round polyimide substrate (inset).