## 5kV multi electron beam lithography MAPPER tool: from 32nm to 22nm resolution capability

<u>C. Constancias<sup>(a)</sup></u>, D. Rio<sup>(a)</sup>, P. Wiedemann<sup>(b)</sup>, B. Dalzotto<sup>(a)</sup>, M. Martin<sup>(a)</sup>, B. Icard<sup>(a)</sup>, L. Pain<sup>(a)</sup>

(a) CEA LETI – MINATEC

CEA-LETI, MINATEC 17 rue des Martyrs F-38054 GRENOBLE cedex9, France

(b) MAPPER Lithography B.V.

Computerlaan 15, 2628 XK Delft, The Netherlands

E-mail address: christophe.constancias@cea.fr

## Preferred presentation method: oral presentation

The maskless lithography is more than ever in the race to provide high resolution patterning capability, (below 22nm), with high throughput for the IC manufacturers. The IMAGINE program led by CEA-LETI in partnership with MAPPER Lithography, ST-microelectronics, TSMC is meant to allow companies to assess a maskless lithography infrastructure for IC manufacturing and the use of MAPPER Technology for high-throughput. This program follows the development of the MAPPER technology up to the beta tool level. It also intends to perform the assessment of this technology and the development of the infrastructure required for its use in manufacturing environment.

A 300mm pre-alpha platform (with 110 beams at 5keV) from MAPPER lithography was installed into LETI mid 2009. Before the next beta tool delivery (mid 2012) with 13,000 beams, the pre-alpha tool has been improved with two main upgrades : projection electron optics getting better resolution capability from 45nm to 32nm; beam switching system allowing the 110 beams to expose separately.

This study will present a short review of the tool status from the acceptance to the last work in progress that includes 32nm half pitch capability. Due to the non conventional acceleration voltage for high resolution lithography, 5keV against 50 to 100keV for standard tools, a study of the exposure parameters' impact has been carried out to optimize the lithography performance: resolution, uniformity and process sensitivity. Several points have been studied:

resist process parameters impact on onset dose and contrast

- tool and exposure strategy to have better results with the actual spot size and backscattering distribution

impact of the stack on backscattering noise

It allowed 27nm half pitch structures to be fabricated (figure 1, figure 2). Exposures and modeling results will be presented and discussed.

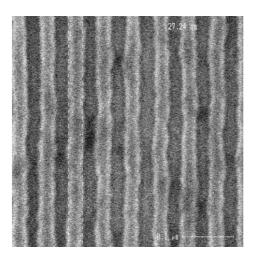


Figure 1 : 27nm half pitch vertical lines, exposed with 5keV MAPPER tool into positive tone chemical amplified resist.

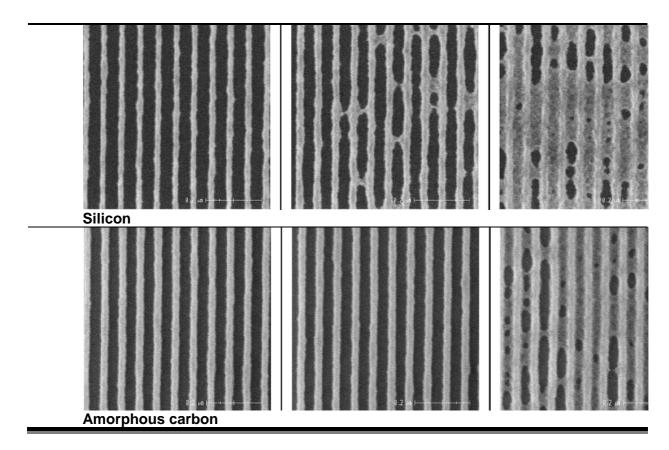


Figure 2 : Improvement of the sensitivity process of the resist, using a 150nm thick amorphous carbon insert between the silicon substrate and resist. Enhancement of the critical dimension, uniformity and roughness for 22nm/64nm pitch with HSQ (negative tone resist)