Development of a 13 silicon suspended stacked nanowire architecture for gate-all-around (GAA) field effect transistors

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Stacked nanowire architectures are well known for being potential solutions for sub-32nm nodes, thanks to their excellent electrostatic control [1-3]. During previous works, we have demonstrated that stacked nanowire metal oxide semiconductor field effect transistors (MOSFETs) with gate-all-around (GAA) or independent double gates (ΦFET) composed of 4 silicon stacked nanowires could be easily achieved. Experiments yielded 18nm stacked nanowire MOSFETs with gate-all-around and for the first time [4-7], we succeeded in achieving sub-20nm ΦFET devices. Electrical results were excellent (ΦFET): for *n*MOS transistors, I_{ON}=6.5mA/µm and I_{OFF}=27nA/µm at an input tension V_{DD}=1.2 V; for *p*MOS, these values are I_{ON}=3.3mA/µm and I_{OFF}=0.5nA/µm (V_{DD}=1.2 V).

Now, we need to improve their current density per layout surface by increasing the number of stacked nanowires. Our challenge was to stack 13 silicon nanowires for the fabrication of GAA transistors. For this purpose, different integration difficulties were overcame especially in lithography and etching. In order to achieve 13 suspended nanowires, we need to pattern a 1µm Si/SiGe multilayer stack via the use of an hybrid lithography (e-beam/DUV) and high selectivity etching processes [6, 7].

For succeeding to etch a 1µm Si/SiGe multilayer stack, a high aspect ratio hybrid resist process was performed (Fig. 1), using the chemically amplified resist NEB22, an ASML stepper (wavelength: 248nm) and a Vistec100KeV vector beam [5-6]. Thanks to this thick resist, we were able to open a 300nm thick oxide hard mask (Fig. 1(D)) keeping the CD bottom of the oxide lines the same as the original lithography CD. Then, the oxide hard mask gave us the opportunity to reach more than 1µm Si/SiGe multilayer stack (Fig. 2(A)) due to an excellent Si/SiGe selectivity to oxide. In order to complete the GAA transistor fabrication, we released silicon nanowires by isotropic etching of the SiGe and we added the gate stack (HfO2/TiN/PolySi) all around silicon nanowires (Fig. 2(B)).

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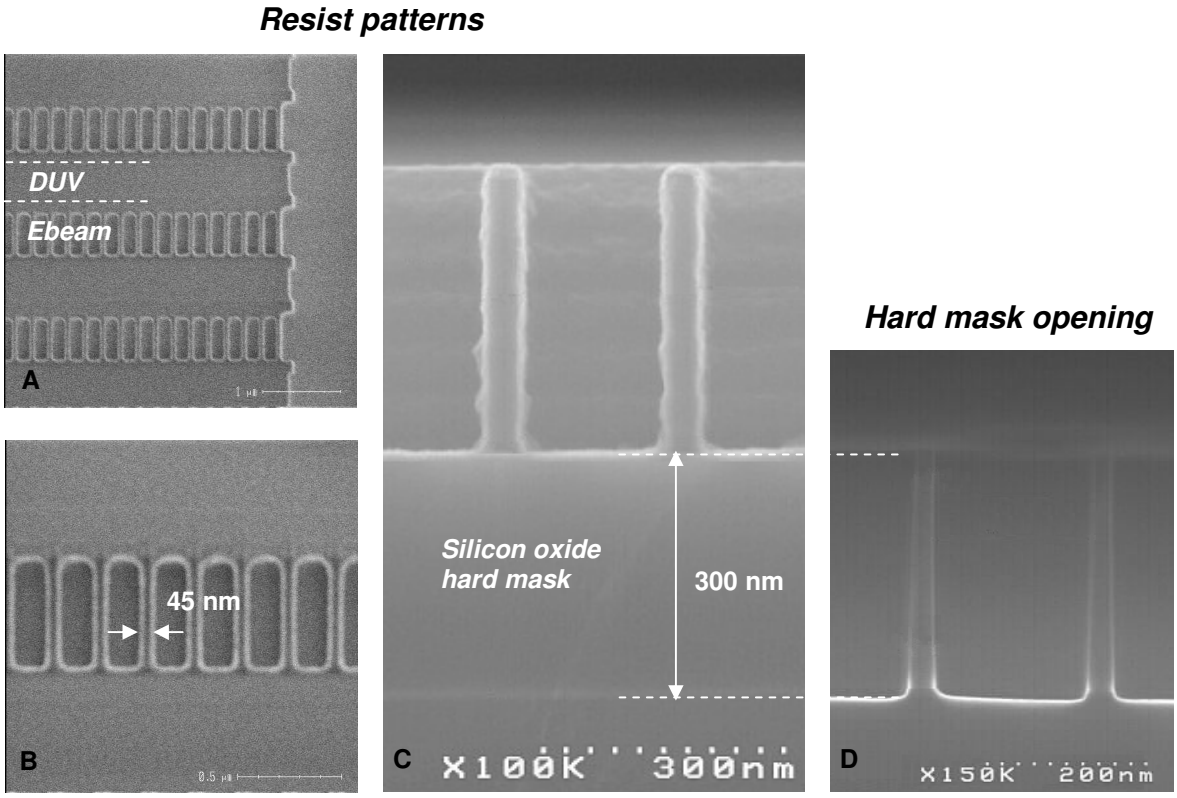

Fig. 1: SEM top view of resist patterns (A, B), cross sectional view of resist patterns (C) and oxide hard mask opening (D)

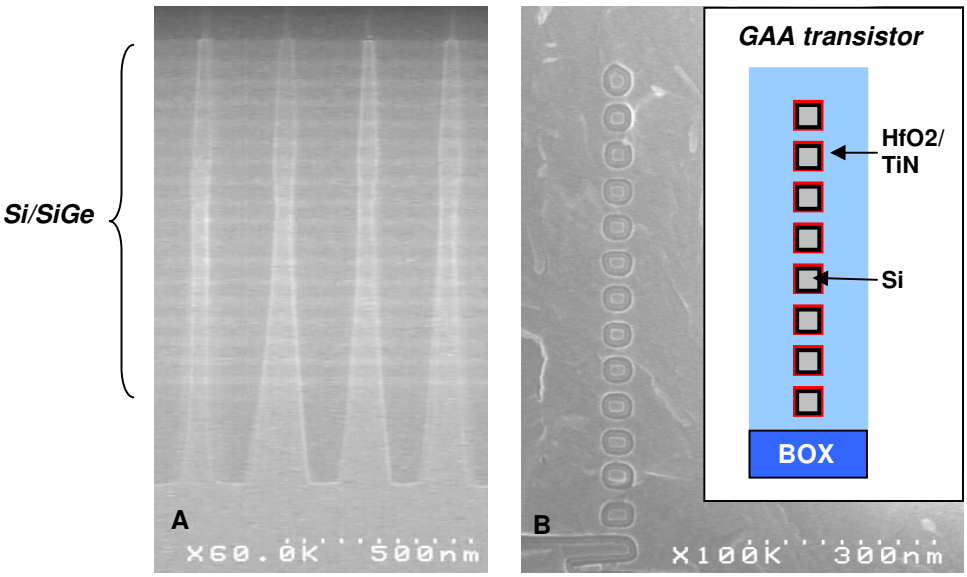

Fig. 2: Cross sectional SEM views of the Si/SiGe stack of 1µm (A), and of the gate all around transistor composed of 13 stacked nanowires (B)