WAFER SCALE INTEGRATION OF ORIENTED CARBON NANOTUBES INTERCONNECTS

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Carbon nanotubes (CNT) are potential candidates for next generation of materials involved in microelectronics devices. In this perspective, it is mandatory to develop new adapted integration protocols. Even if CNT have been integrated as transistors, sensors, interconnections and other devices [1, 2], patterning techniques capable of wafer scale integration still have to be developed. In this contribution, we present dielectrophoretic manipulations of CNT that turned out to produce oriented CNT patterns over large surfaces.

PECVD techniques and patterns of engineered catalysts can be used to locally grow dense bundles of CNT. The control of the quality of the CNT and the high synthesis temperature required are the main problems of these techniques for integration purposes in microelectronics processes. Another possibility is to synthesize and purify high quality CNT prepared *ex situ* and integrate them on the devices. This method allows the control of the electrical and physical properties of CNT before their integration. They can be purified, sorted and functionalized depending on the requirements of the targeted devices. One of the main bottlenecks of these techniques is the control of the orientation of those highly anisotropic nano-objects at the wafer scale. We have developed a versatile technique using electrical fields and capillary forces control. The method is specifically efficient for generating oriented and precisely localized interconnections at the wafer scale.

The protocol is based on dielectrophoresis manipulations using buried electrodes. Two gold electrodes are designed to create strong electrical fields at very precise locations and over large arrays. The electrodes are then covered with a thin (300nm) insulating layer (Silicon Nitride or resist). Then, a drop of purified CNT suspension obtained by CCVD technique [3] is deposited and an adapted electrical bias is applied between the electrodes using a function generator. The insulating layer avoids any contact between the CNT and the dielectrophoresis electrodes and prevents CNT to be stuck on the electrodes or to be damaged by a strong current. The next step is a careful pull out of the droplet from the insulating layer to avoid any disorientation of the CNT due to the capillary forces which are quite strong on the triple line (substrate/liquid/air). Using this technique, dense bundles of oriented CNT can be precisely localized and oriented at the wafer scale. Depending on the applications, the CNT can be then transferred on another substrate by contact printing or directly used to connect individual pair of electrodes. A typical result of individual interconnections is shown on the SEM picture of figure 1 and an example of a statistical analysis of the resistance of such connections at a wafer scale (4 inches) is presented on figure 2.

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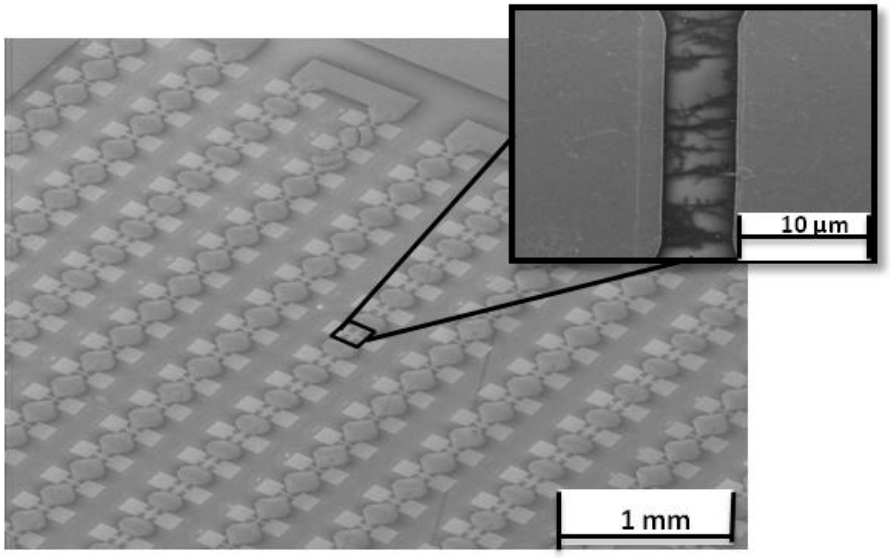

Figure 1: SEM image of the produced CNTs interconnections at a wafer scale. The in plane electrodes are thin Ti/Au electrodes obtained by lift-off. The buried electrodes are used to create strong localized electrical fields and the top electrodes are used to test at the wafer scale CNTs interconnections. The CNTs are visible in the inset (darker lines) between two gold electrodes.

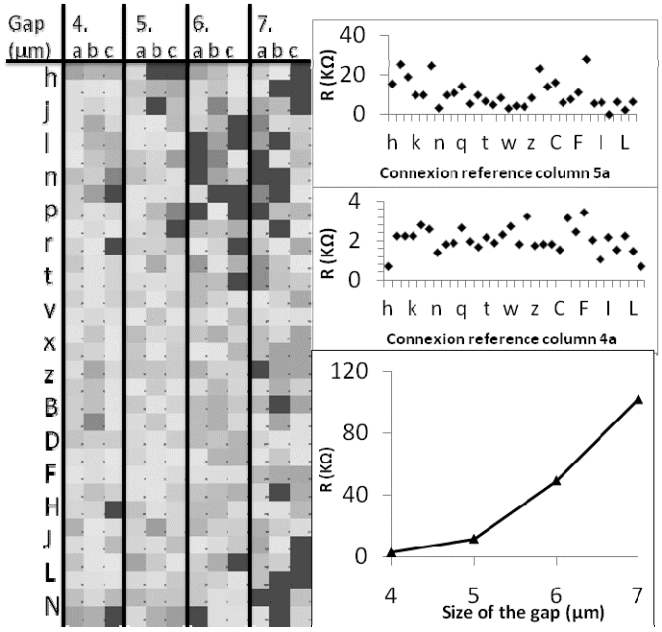

Figure 2: Example of statistical analysis on a large array of CNTs interconnections. The table is an analysis of the resistivity dispersion in grey scale. The graphs illustrate studies of the resistance homogeneity on the same geometry of connected electrodes and a study of the evolution of the average resistance as a function of the size of the gap between the electrodes. Note the predominant metallic behavior of our Double wall CNTs.