Novel method for fabrication of Nanoscale Single-Electron transistors: Electron beam induced deposition of Pt and atomic layer deposition of tunnel barriers

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We propose and demonstrate a novel method for fabricating metal-based single-electron transistors (SETs) that combines a nanoscale island produced by electron beam induced deposition (EBID) of metal with a tunnel barrier dielectric produced by atomic layer deposition (ALD). Electron beam induced deposition of materials was recognized as a promising method of nanofabrication capable of producing features down to a few nm in size. As deposited, EBID metals are intermixed with highly resistive amorphous carbon [1] resulting in an insulating state at low temperature. A post-deposition anneal in O_2 ambient increases the grain size of the metal and removes the majority of carbon residue, reducing the resistivity of the EBID nanostructures by several orders of magnitude [2,3]. Pt/C nanostructures were deposited in FEI Helios NanoLab 600 system using $C_9H_{16}Pt$ gas as a precursor. Using a 2 minute anneal in O_2 ambient we achieved metallic behavior at low temperatures ($R_\square$ <0.5 k$\Omega/\square$). Figure 1 shows a micrograph of a test line after anneal.

In a SET the EBID metal island must be separated from source and drain wires by tunnel barriers. The ALD technique opens up a way to produce high quality tunnel barriers with atomic precision and significantly reduce the number of charge defects causing random background charge fluctuations in SETs. The optimal thickness of the tunnel barrier (12 ALD growth cycles) was experimentally determined to obtain a junction resistance ~ 1MΩ.

Circular-shaped islands, 50 to 100 nm in diameter, were formed using EBID between the source and drain wires that were coated with ALD film of Al_2O_3 (Fig. 2). Devices were tested at low temperature and show characteristic features of Coulomb blockade (Fig. 3) that are consistent with the obtained overlaps between the wires and the island. We need to note that the value of charging energy will be significantly increased by optimizing these overlaps.

Unlike a previously reported observation of single-electron transistors using EBID [4-6], our fabrication method offers tight control of the crucial element of the SET fabrication, the nanoscale tunnel junctions. This opens a path to a fabrication method to produce SETs with the desired island geometry, possibly in a form of 3D structures (e.g. bridges). However one fabrication obstacle has to be resolved: the deposition of conductive "halo" visible in Figure 1 and 2, surrounding the EBID materials greatly reduces coupling to the gate and acts as "shielding media" capable of random charging. We are currently investigating methods of resolving this issue.

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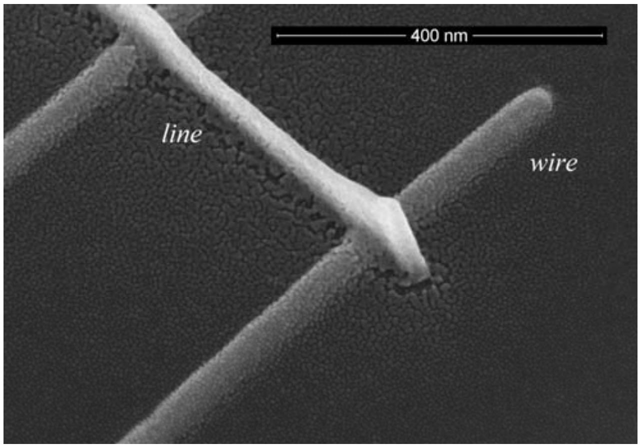

Figure 1. Micrograph of Pt/C test "lines" deposited on top of thin (5 nm/20 nm) wires (Ti/Pt) patterned by e-beam lithography and metal deposition to form source and drain electrodes for both test structures, lines and SETs. Oxidized Si wafers are used as substrates

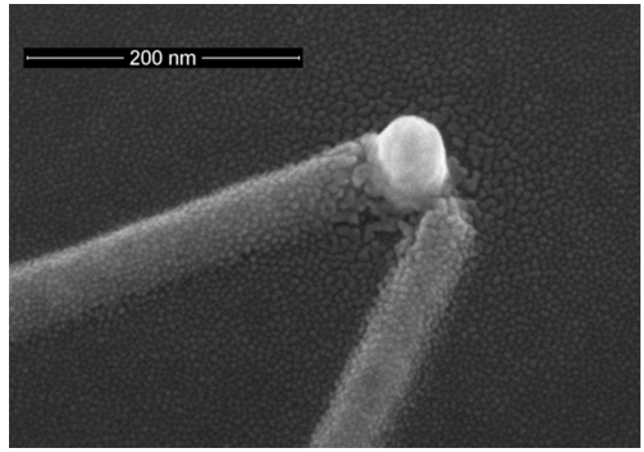

Figure 2. SEM micrograph of the SET device. The island is deposited on top of ALD dielectric. "Halo" composed of residual metal particles is clearly visible

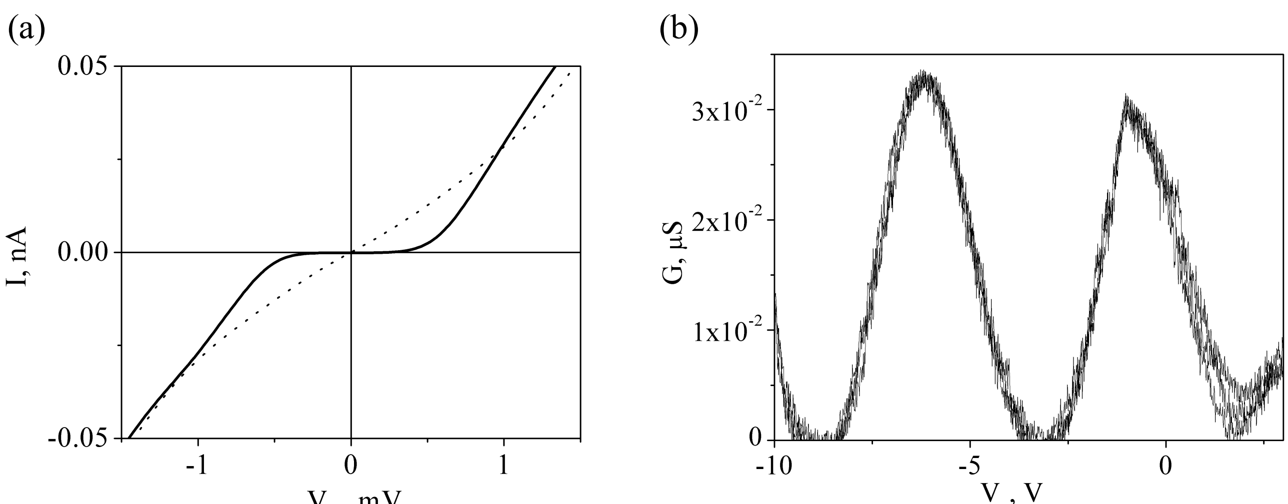

Figure 3. (a) I_{ds}-V_{ds} characteristics of the SET #1 with Coulomb blockade lifted (dashed line), and in full blockade (solid line). The charging energy, $E_C \approx 0.5$ meV. T=0.3K (b) Coulomb blockade oscillations in SET #2 at 0.3K. Three successive scans are shown