Fabrication of Hybrid Silicon/Metal Island Single Electron Transistors

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We have previously demonstrated a novel process for Silicon Single Electron Transistors (Si-SET) with a high charging energy (~20 meV), combining Chemical Mechanical Polising (CMP) with the advantages of silicon processing [1]. However, the Si-SET also exhibits numerous anomalies related to the random dopants in the silicon island and the leads. We report the results of a new process variation: replacing the silicon island with aluminum, to reduce or even eliminate the doping effects in Si-SETs.

In Fig 1, a degenerately doped silicon on insulator (SOI) wire (~15 nm) is embedded in planarized oxide using nano encapsulation technique as reported in [1]. During the plasma etching of the SOI, the low bias over-etch step is extended to sufficiently undercut the silicon to suspend the wire. Using Electron Beam Lithography (EBL), a pit (~25 nm) is selectively etched in an Inductively Coupled Plasma (ICP) to separate the wire (Fig 2.) A tunnel oxide (1.5nm) is formed on the sidewall of the pit by rapid thermal oxidation (RTO) followed by metal evaporation. The metal overburden is removed by CMP, leaving the metal in the pit to form the SET's island.

CMP's susceptibility to metal dishing and erosion can prevent the aggressive over-polishing needed for complete removal of metal residue outside the pit and for thinning-down the SETs. We developed a technique to selectively remove these metal residues by adding a capping layer and varying the CMP process to change the selectivity between metals and oxide. In Fig 3, the thickness of the deposited aluminum is less than the depth of the pit so that the capping layer can also be below the top of the pit. Outside the pit surface roughness, caused by issues such as the oxide loss during the ICP silicon etching, has a much shallower depth (~ 20nm) and is filled only with aluminum. To demonstrate the process, Al and cap metal were deposited on test patterns (tens of microns in size) that are much larger than the topography (low aspect ratio). Reducing the oxidant in a slurry that targets aluminum, reduces the capping layer polishing rate significantly in the over-polish step. Since the capping layer protects the aluminum in the pit, dishing is dramatically improved across the entire sample. Although the metal to oxide selectivity decreases slightly with less oxidant, the SET can be thinned down gradually to reduce the size of the island.

At room temperature both the SET and the dummy line behave as resistors: 210 kΩ and 8 kΩ, respectively. At lower temperatures, a strong non-linearity in conductance (Fig.5) indicates possible Coulomb Blockade (CB), while the dummy line stays metallic. The dummy line resistances were compared before and after the CMP to estimate the remaining thickness of the wire, ~35nm, which implies a charging energy E_C~3 meV based on the junction capacitance of this size. In Fig 6, the >50% peak-to-valley ratio of the conductance oscillation at 4K suggests E_C>1meV, in accordance to our expectation. The SET is not very stable with "jumps" and shifts in conductance observed during the measurement. This is a common phenomenon with SETs suffering from background charge fluctuations.

[1] Lee et al., "Si single electron transistor fabricated by chemical mechanical polishing," J. Vac. Sci. Technol. B 28, C6L9 (2010)

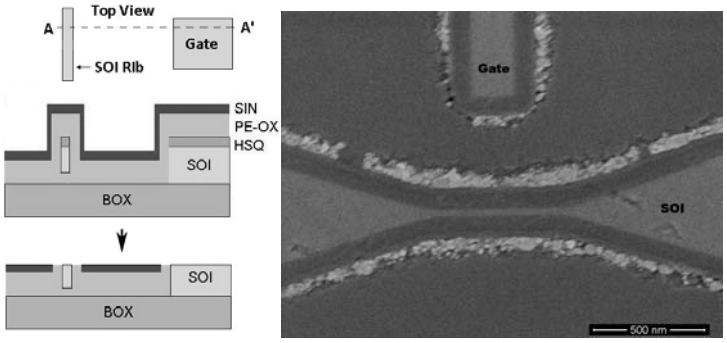


Fig. 1 Suspended SOI line (15nm in width) is defined using EBL, embedded, and planarized in oxide CMP. The rubbles in the SEM image are the sidewall roughness from PECVD oxide deposition.

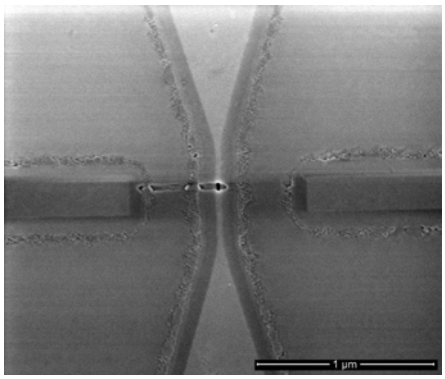
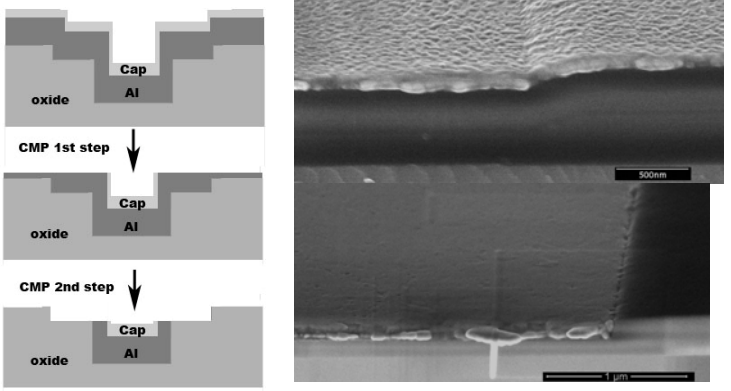


Fig. 2 A pit (~25nm) is etched to separate the wire. The oxide is slightly etched as well (<20nm) by the ICP.



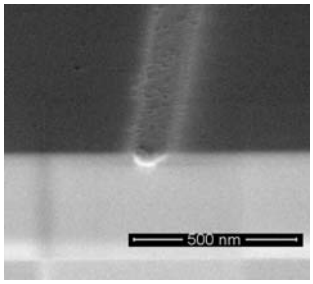


Fig 3. Al CMP. The 2nd Step has a slow polishing rate on the capping layer. A much longer over-polished is possible to ensure the removal of Al residue. The upper SEM image shows the as-deposited metal/cap layer thickness matches the height of the topography (120nm). After CMP, no dishing is observed (bottom SEM). An Al wire (~80nm in width) is embedded in oxide using the same technique.

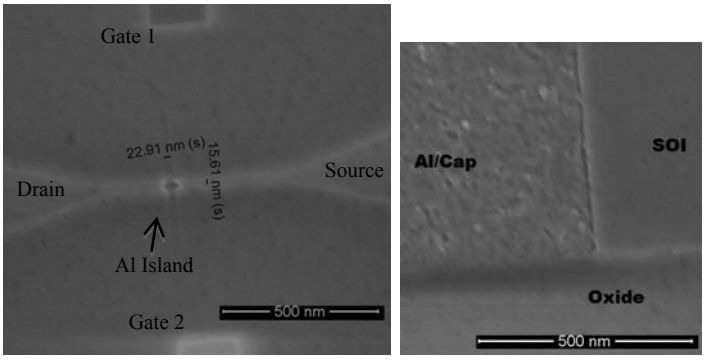


Fig 4. SEM images taken after the process is complete. (Left) The SOI line (15nm) is separated by a pit (23nm) where the island is located. (Right) The test pattern on the same sample showing the region where the SOI was etched is now filled with aluminum, and there is no sign of metal staining on the silicon or oxide that might cause electrical shorts.

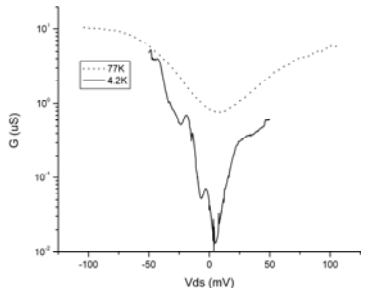


Fig 5. SET conductance at 77K and 4.2K

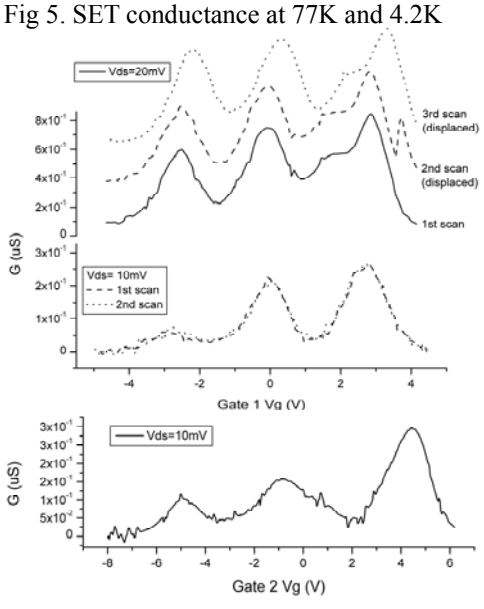


Fig 6. Conductance oscillates versus the gates voltage. Shifts and "jumps" of these peaks were observed during the measurement. At V_{DS}=20mV, the data from the second and the third scans of the V_{DS} are shifted upward for clarity. Similar oscillation is obtained using the other weaker gate.