Memory characteristics of MOS capacitors with Pt-nanoparticles-embedded gate layers

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Recently, room-temperature processable fabrication for nonvolatile memory devices has attracted considerable attention since plastic based devices considered as one of promising next-generation devices are vulnerable to heat [1~3]. Especially, nano-floating gate memory (NFGM) structures containing nanoparticles embedded in gate layers have been fabricated using nanoparticle synthesized in solution at room temperature[4,5]. However, solution processable fabrication meets a hindrance to solve for reproducibility. Therefore, in this study, we propose new room-temperature processable fabrication for NFGM by utilizing Pt nanoparticles (NPs) sputtered in system with a cooling unit.

Pt NPs were formed on SiO_2 layers with a thickness of 6.3 nm on top of silicon (p-type, (100)) wafers by DC magnetron sputtering method and the SiO_2 layers were used as the tunneling oxides. Control oxide layers of SiO_2 with a thickness of 35 nm were then deposited by RF magnetron sputtering. Subsequently, top electrodes of Au were deposited on the control oxide layers by thermal evaporation. The structure and electrical characteristics of our devices were examined with transmission electron microscope (TEM) and a semiconductor parameter analyzer, respectively.

Figure 1 shows cross-sectional TEM images of MOS capacitors with Pt-NPs-embedded gate layers. The sputtered Pt NPs with an average size of 4 nm diameter are formed isolatedly from each other between the tunneling and the control oxide layers. The capacitance versus voltage (*C*-*V*) curves obtained at 1 MHz are exhibited in Fig. 2. The flat-band voltage shift of 2.8 V is observed in a counter clock wise direction when voltage is swept from +10 to -10 V, indicating the storage of injected holes on Pt NPs.

References

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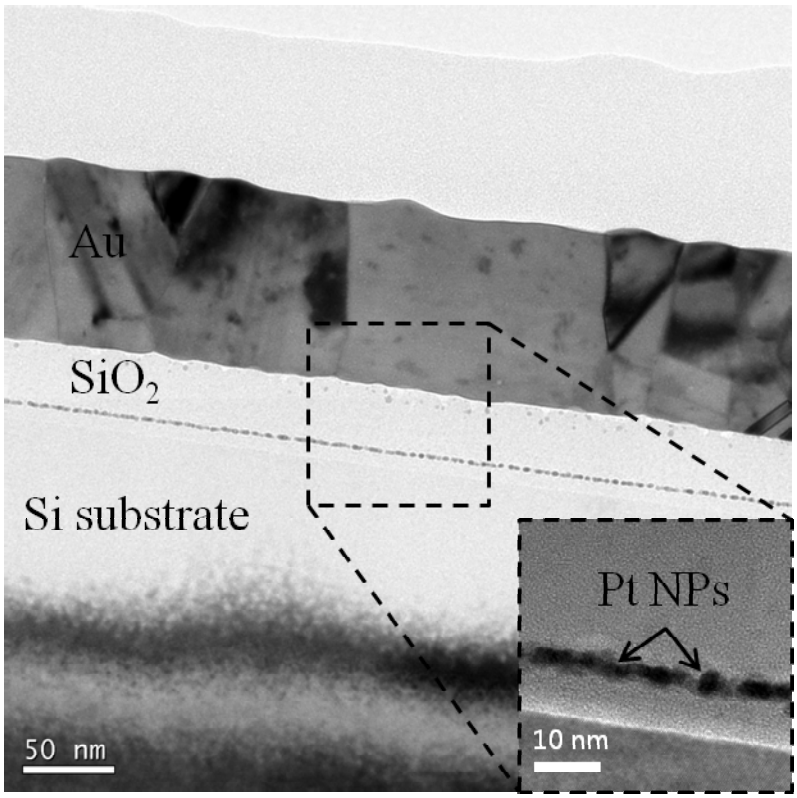

Figure 1: Cross-sectional TEM Images of a MOS capacitor with a Pt-NPs-embedded gate layer

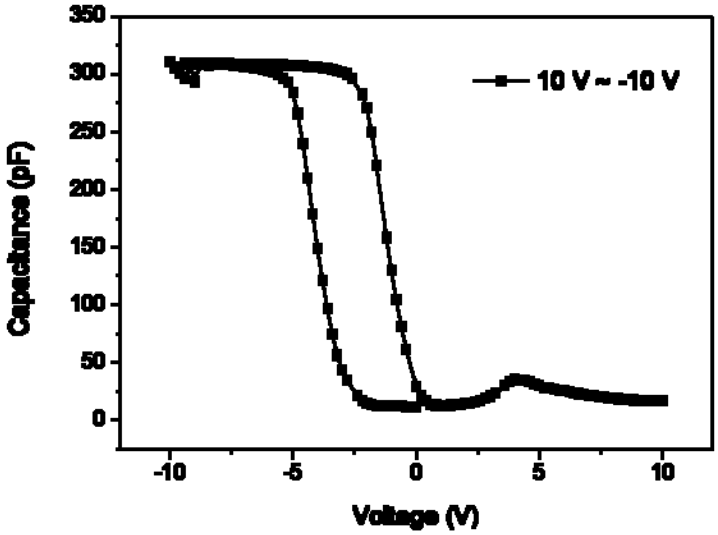

Figure 2: High -frequency C-V curves of a MOS capacitor with a Pt-NPs-embedded gate layer