Nanofabrication of High Aspect Ratio Nanoscale TSVs

A. Dembla, D.K. Brown and M.S. Bakir
Nanotechnology Research Center,
Georgia Institute of Technology, Atlanta, GA 30318
adembla@gatech.edu

Through Silicon Vias (TSVs) is a rapidly emerging technology in silicon nanoelectronics. Technology scaling to sub 22nm node provides more efficient and complex functional systems with higher bandwidth and throughput. Electrical connectivity limits the performance of such systems. Scaling interconnects often leads to difficulties due to increased resistance as a result of several scattering mechanisms[1]. This limits the 2D connectivity of high performance ICs and hence their capability. Monolithic 3D integration has shown high integration densities, but is limited by the thermal budget and power density limits. In this work, we propose a vertical interconnect technology that is dimensionally comparable to conventional 2D (metal 1 like) interconnects and hence offers an extremely high integration density ($>10^8/cm^2$).

To demonstrate the feasibility of the proposed idea, three main issues need to be addressed namely nanolithographic patterning, etching TSV & copper filling TSVs. These processes are well addressed in literature for via diameters greater than 0.5 micron (Ref. 2). In this work, a demonstration addressing the above three issues is shown for via diameter of 100 nm. Electron beam lithography (JEOL JBX-9300FS) was used to pattern arrays of 100nm/200nm/500nm (diameter) vias on ZEP, that is used as a photoresist as well as an etch mask. The patterns were developed in amyl-acetate and cross section imaging was done, as shown in Figure 1. By using the Bosch process on the STS ICP the vias were etched with aspect ratio of ~18:1. ZEP shows a good etch resistance to the ICP process with a selectivity of 10:1 against silicon. The etch rate shows direct correlation with via diameter, this leads to constant aspect ratio etch for fixed number of etching-passivation cycles. The etch process for these TSVs has been optimized to minimize the taper which can increase TSV resistance by 4x for a taper angle of one degree. The optimized process has a taper angle of 0.4 degrees as shown in figure 2. Bottom up copper plating is demonstrated for TSVs with diameter of 100nm and height of 2um (Figure 3). The electroplating was performed in a standard copper bath at room temperature, using copper plating solutions.

The nanoscale TSVs demonstrated as a part of this work can potentially enable the emerging high bandwidth and high performance systems as well as the low capacitance interconnects needed for nanophotonic integration. By performing electrical and reliability measurements, the fabricated TSVs can provide valuable data to validate the scalable models proposed in published literature[3].

[1]D. Josell, S.H. Brongersma, and Z. Tőkei, Annual Review of Materials Research, 39, (2009)
[2]X. Wang, W. Zeng, and E. Eisenbraun, J. Micromech. and Microengg., 17, (2007)
[3]D. Khalil Y. Ismail, M. Khellah, T. Karnik and V. De, 9th ISQED, 2008

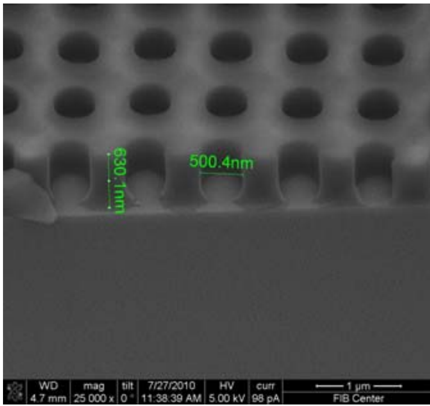

Figure 1: Cross-section image of 500nm patterns in ZEP (Dose: 240uC/cm^2).

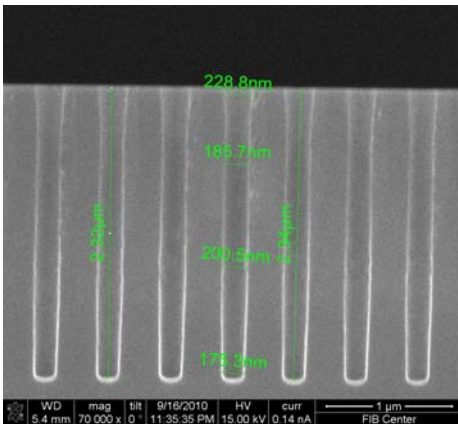

Figure 2: Taper in 200nm diameter blind TSVs.

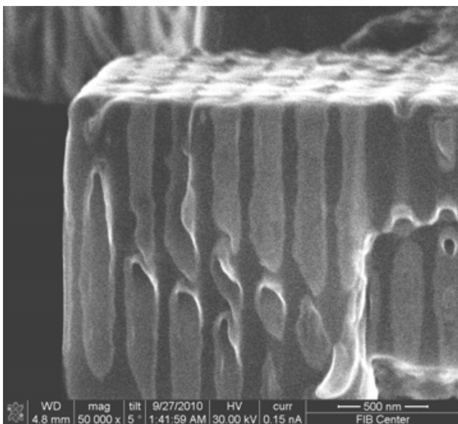

Figure 3: FIB cross-section image of copper plated 100nm TSVs (discontinuity is an artifact of the FIB).