Double-Surrounding-Gate MOSFET: Enabling Robust Process Control at Deep Nanoscale

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As MOSFETs are scaled down to sub-15 nm, the transistor structure has evolved from the single-gate to multiple-gate schemes as shown in Fig. 1 [1, 2]. There are many multiple-gate schemes, while their fabrication challenges are quite different. For example, a vertical double-gate MOSFET encounters severe fabrication difficulties in patterning a thin and high-aspect-ratio body. Also, a vertical (surrounding-gate) nanowire transistor suffers from similar problems as it is difficult for sub-15 nm tall Si pillar structures to survive in etching and cleaning processes. This is why FinFET is considered to be more manufacturable as its thin channels are horizontally sandwiched between source and drain, which helps to form mechanically stable structures. Nevertheless, a horizontal design such as FinFET sacrifices the transistor density and it is always attractive to search for a vertical design which can avoid the challenges of patterning small and high-aspect-ratio 1-D or pillar structures.

In this paper, we propose a vertical double-surrounding-gate (DSG) MOSFET to overcome above technological challenges (Fig. 2). The advantages of a DSG MOSFET are mainly because it allows higher transistor density, significantly improved device immunity to CD variation, using the spacer technology to pattern small and uniform (circular) body with a high aspect ratio, and excellent gate control.

The fabrication process to pattern a circular body using the spacer technology is shown in Fig. 3. First, a sacrificial pillar structure is patterned, with its diameter significantly larger than what would be required if this pillar was directly used as the MOSFET body. Usually, both mechanical stability and CDU of large pillars are better than small pillars. After that, a thin spacer can be formed around the pillar structure followed by the sacrificial release using a highly selective etching process. The left circular structure will be used as a hard mask to pattern the body film stack underneath such that a mechanically stable body can be formed. The main issue is the variation of the channel area (perpendicular to the current direction) due to the radius non-uniformity of Si cylinders. However, the significance of CD non-uniformity of Si cylinders is quite different for nanowire and DSG MOSFETs. If the DSG body thickness t is comparable to the body radius r of a nanowire, the caused (percentage) variation of the DSG channel area will be about 1/3 of a nanowire MOSFET.

We shall analyze nMOSFET with lightly doped p-type Si (or undoped) body, but the results are applicable to pMOSFET and other material as well. The 1-D Poisson's equation is [1]: $\frac{d^2\varphi}{dr^2}+\frac{1}{r}\frac{d\varphi}{dr}=\delta\frac{kT}{q}e^{\frac{q(\varphi-V)}{KT}}$. The symbols follow those widely used in the literature of compact device modeling [1, 2]. Theoretical break-through has been made recently to analytically solve the nonlinear Poisson's equation in the cylindrical coordinate. The general solution of Poisson's equation is [2]: $\varphi(r)=V+\frac{kT}{q}[(A-2)\ln r-2\ln(r^A-B)+\ln(\frac{2BA^2}{\delta})]$ where A and B are two integration constants to be determined from two boundary conditions. The induced inner and outer charge density are related to the surface electric fields by Gauss's law:

$$Q_{i1} = -C_{ox1}(V_g - \Delta\phi - \varphi_{s1}) = \varepsilon_{si}\frac{d\varphi}{dr}(r = r_1) = \varepsilon_{si}\frac{kT}{q}(\frac{A-2}{r_1} - \frac{2Ar_1^{A-1}}{r_1^A - B})$$

$$Q_{i2} = -C_{ox2}(V_g - \Delta\phi - \varphi_{s2}) = -\varepsilon_{si}\frac{d\varphi}{dr}(r = r_2) = -\varepsilon_{si}\frac{kT}{q}(\frac{A-2}{r_2} - \frac{2Ar_2^{A-1}}{r_2^A - B})$$

Given the gate voltage, we can use above two equations to numerically solve two integration constants $A(V)$ and $B(V)$ as functions of quasi-Fermi potential V, and the induced inversion charges $Q_{i1}(V)$ and $Q_{i2}(V)$. The drain current can be calculated using Pao-Sah's integral:

$$I_{DS} = \mu\frac{2\pi r_1}{L}\int_0^{V_{DS}} Q_{i1}(V)dV + \mu\frac{2\pi r_2}{L}\int_0^{V_{DS}} Q_{i2}(V)dV = \mu\frac{2\pi r_1}{L}\int_{A_1}^{A_2} Q_{i1}[A, B(A)]\frac{dV}{dA}dA + \mu\frac{2\pi r_2}{L}\int_{A_1}^{A_2} Q_{i2}[A, B(A)]\frac{dV}{dA}dA$$

A_1 and A_2 are the values of A corresponding to $V = 0$ and $V = V_{DS}$ respectively, L is the channel length, and μ is the carrier mobility.

Numerical calculation of two integration constants A and B is non-trivial as both of them can be complex numbers. The success criterions include: there should be no discontinuity/infinity point in electric field whose sign on both surfaces must be consistent. Also, the resultant potential should have negligible imaginary part. It is found that the concentration of induced inversion charge in an undoped (or lightly doped) body of a DSG MOSFET is comparable to a conventional double-gate device (Fig. 4), indicating an excellent gate control to reduce leakage current is achievable by a DSG MOSFET.

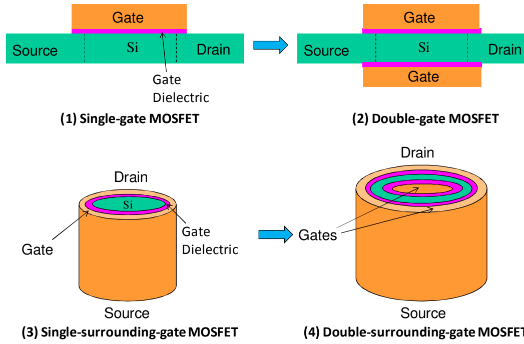

Fig. 1. Evolution of MOSFET structure.

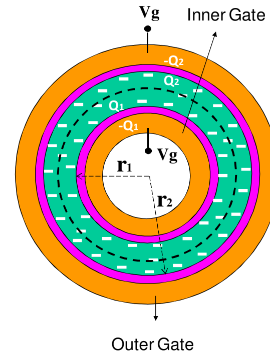

Fig.2. The cross-section (perpendicular to current direction) view of a DSG body.

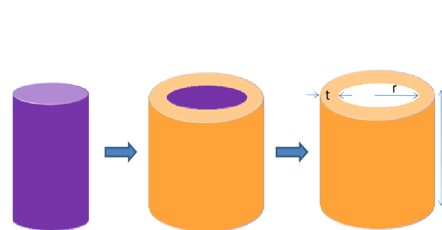

Fig. 3. A spacer process to fabricate a circular DSG body.

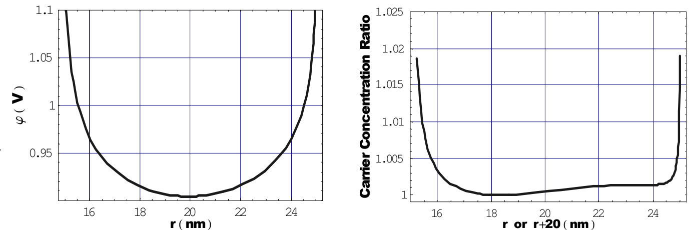

Fig. 4. The potential distribution in a DSG body (left), and a comparison (right) with a double-gate device under the same boundary conditions.

References

[1] Y Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge, U.K., Cambridge Univ. Press, second edition, 2009.

[2] Y. Chen, "Nanodot and nanowire transistor device modeling and fabrication process," *Jpn. J. of Appl. Phys.*, Vol. 46, No. 9B, pp. 6213-6217, 2007.