Fabrication of silicon template with smooth tapered side wall for Nanoimprint lithography

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Nanoimprint lithography is an attractive technology for the fabrication of diffraction unlimited patterns due to its low cost and high throughput. In Nanoimprint lithography the patterns in a template are first transferred to a resist film. After the resist is cured, the template has to be released from the resist film. In order to release the template from the resist, a demolding force is required. When the template strongly sticks to the resist film, the releasing process cannot be completed successfully and transferred resist patterns must be damaged. It is very important to fabricate templates with suitable etching profile. Namely a smooth tapered side wall is necessary, in order to reduce demolding forces [1]. Furthermore, an underetching should be avoided. In this work we developed an RIE etching process to fabricate silicon templates with smooth tapered side walls for Nanoimprint lithography. In this etching process a dual layer etching mask was used to avoid underetching. Electron beam lithography was used to define the patterns in the resist. The etched structures have lightly tapered side walls and a surface roughness of less than 5 nm. The side wall angle can be controlled from 90° down to 85° by variing the ratio of etching and passivation gas. Using this etching process we successfully fabricated silicon structures with sizes down to 50 nm and aspect ratios up to 10. The etching rate is more than 100 nm/min. Using this silicon template with smooth tapered side walls the demolding force in Nanoimprint lithography can be dramatically reduced.

[1] H. Schift and L.J. Heyderman, Alternative Lithography. In: C.M. Sotomayor Torres, Editor, Kluwer Academic/Plenum Publishers (2003), p. 47.

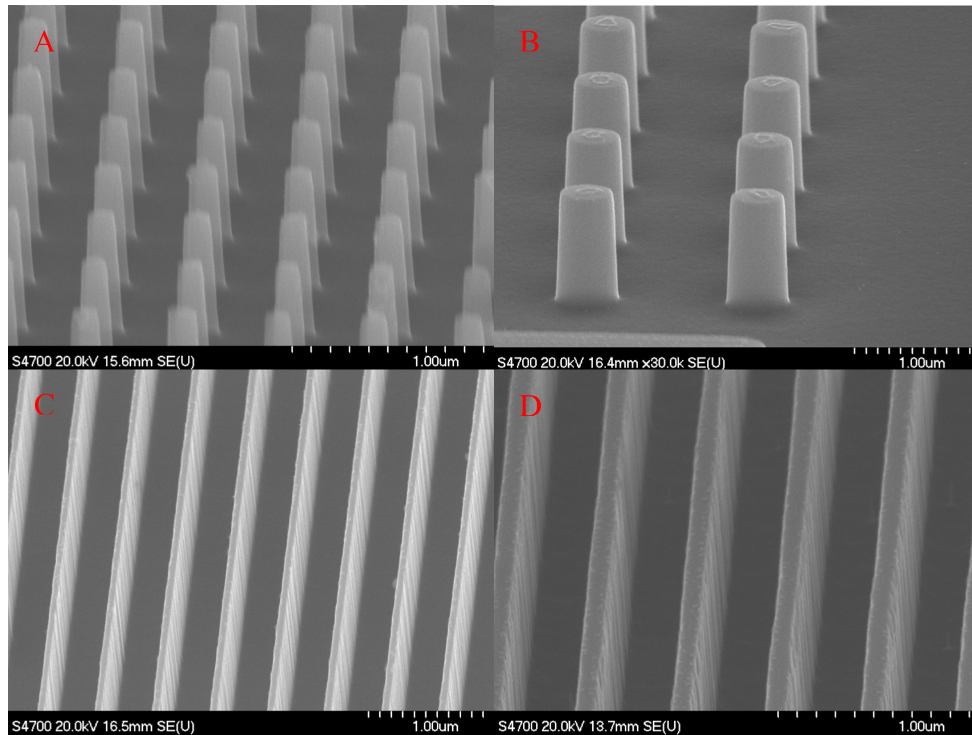

Figure 1: SEM image, 30 ° tilted, lines and pillars etched with the etching process developed in this work: A): Pillar array, 100 nm diameter, 800 nm high, side wall angle 85 °. B): Pillar array, 300 nm diameter, 1000 nm high, side wall angle 85 °. C): Line array, 50 nm line, 450 nm space, 800 nm high, side wall angle 85 °. D): Line array, 100 nm line, 400 nm space, 800 nm high, side wall angle 85 °.