Challenges in Data treatment and Proximity effects correction for massively parallel electron lithography

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Lithography faces today many challenges to meet the ITRS road-map. 193nm is today the only existing industrial option to address high volume production for the 22nm node. Nevertheless to achieve such a resolution, double exposure will be mandatory for critical level patterning. EUV lithography is still challenged by the availability of high power source and mask defectivity and suffers from a high cost of ownership perspective [1]. Its introduction is now not foreseen before 2015.
Parallel to this mask-based technologies, mask less lithography regularly makes significant progress in terms of potential and maturity. The massively parallel e-beam solution even appears as a real candidate for high volume manufacturing [2-3]. Several industrial projects are under development, one in the US, with the KLA REBL project and two in Europe driven by IMS Nanofabrication (Austria) and MAPPER (The Netherlands). The way to industrial maturity is still long for maskless lithography, as current development is still on the path for the first alpha tools.
Among the developments to be performed to secure the take off of the multi-beam technology, the availability of a rapid and robust data treatment solution will be one of the major challenges. The main data manipulation step consists in converting from GDS or OASIS file format into the tool proprietary format, including all potential proximity effect corrections. This has to be performed reliably and quickly. This paper will detail this process and identify the key challenges in terms of specification, speed and accuracy. It will focus on results obtained using a MAPPER tool within the IMAGINE program driven by CEA-LETI, in Grenoble, France. A status on the development work already done will be presented. As an illustration, Figure 1 shows a comparison between a lithography performed on the MAPPER tool with or without E-Beam Proximity Correction (EBPC) on a 32nm SRAM. The software platform Inscale from Aselta Nanographics was used to perform the data processing including the dithering and proximity correction. After correction, every feature can be perfectly delineated. On the active level shown in Figure 2, the difference in CD between the center and the edge of the device is reduced from 10nm to 0 using EBPC. Finally, the paper will help to get a better understanding of the work still to be done to be on time to meet the maskless lithography challenge.

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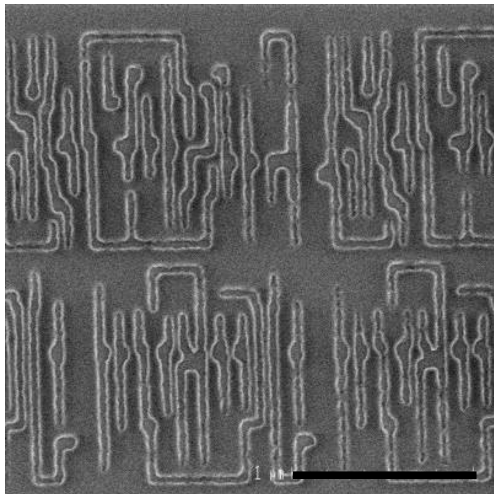
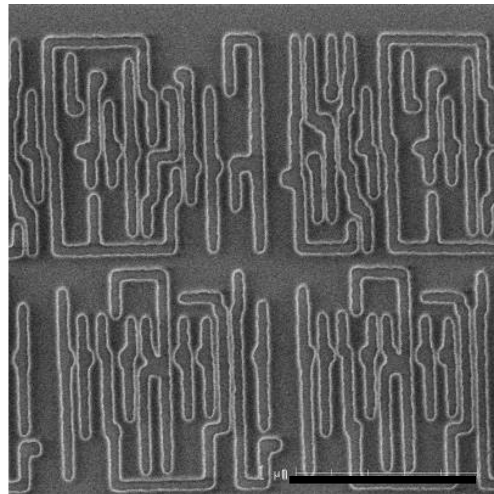
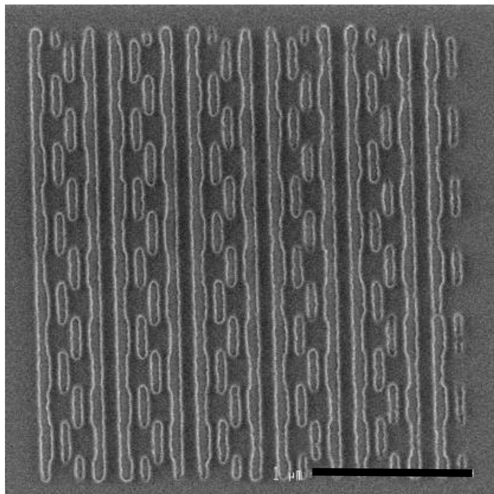
[2] C. Klein et al., Projection maskless lithography (PML2): proof-of-concept setup and first experimental result, Proc. SPIE 6921, 2008.
[3] V. Kuiper et al., Mapper: high throughput maskless lithography, Proc SPIE, 7470, 2009

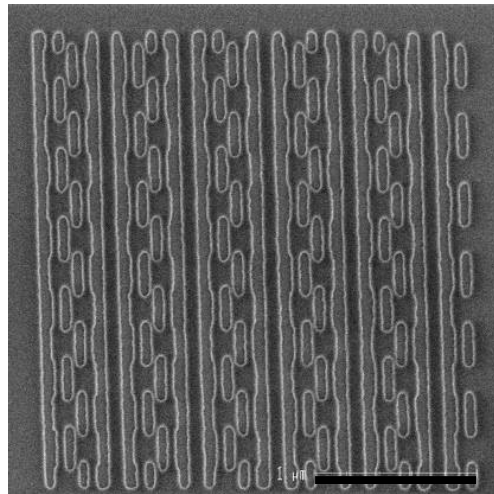




(a) (b)

Figure 1 : Poly layer of a 32 nm SRAM exposed using the Mapper tool (a) without correction and (b) with proximity correction. The black bar is 1µm.





(a) (b)

Figure 2 : active layer of a 32 nm SRAM exposed using the Mapper tool (a) without correction and (b) with proximity correction. The black bar is 1µm.