Neon GFIS Nanomachining Applications –A study of the machining properties of Neon for Semiconductor FA and Circuit Edit

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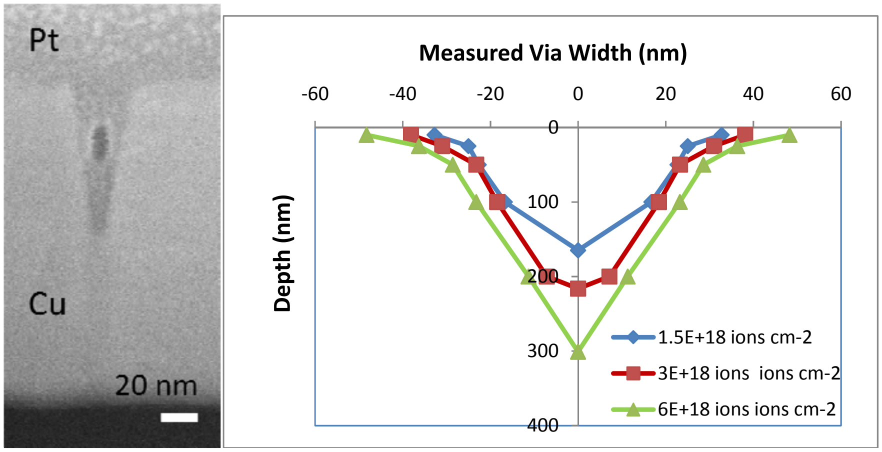
In January, 2011 Intel's debuted its latest generation microprocessor, code named Sandy Bridge™, at the Consumer Electronics Show. This is the second generation of processors built on Intel's 32 nm process node [1]. Continuing with a two year cadence of products being released on new process technologies, we can expect to see microprocessors built on sub 10 nm process within the next 5-6 years. Shrinking transistor dimension and advances in device layers enables better computing performance, but it poses challenges for semiconductor analysis, particularly in the areas of Nanomachining required for fault isolation, TEM prep, and backside circuit edit.

Gallium liquid metal ion source (LMIS) technology is the most commonly used charge particle beam for the focused ion beam (FIB) industry in the past few decades. While R&D efforts continues in scaling the gallium beam spot size; various alternative charged particle beam technology innovations have been put forth by researchers around the world, e.g., helium and neon gas field ionization source (GFIS), lithium and chromium magneto optical ionization source (MOTIS), multicusp plasma ion source, and alloy liquid metal ion source [2-5].

As the transistors shrink in geometry, it is critical to scale the ion beam probe size to increase the image resolution to resolve features in the circuitry to be modified during TEM prep or nanomachining. Neon GFIS has demonstrated better than 1 nm resolution. But is having a small probe size enough? It is increasingly more important to have a shallower damage layer during TEM sample prep and have capability of accessing a small node without damaging adjacent devices during backside circuit edit. From various experiments and simulations, it is clear that besides probe size, other factors must be considered, e.g., current distribution within the beam, sputtered atom lateral distribution, beam energy, beam material interaction, subsurface damage density and distribution, sputter yield, beam tail interaction with gas chemistry, scattering of the ion beam in the chamber, etc.

In our previous work, neon GFIS sputtering and beam material interaction characteristics were thoroughly analyzed on different semiconductor materials; both in imaging dose region and nanomachining dose region [6]. In this paper, we will discuss major considerations in charged particle beam development for circuit edit, TEM, and FA nanomachining applications. We will provide a quantitative comparison between the latest experimental results (figure 1) and the theoretical expectations (figure 2). Data to be presented includes nanomachining sputter profiles for sub 100nm FIB via applications, impact of subsurface damage on machining, and sputter distribution effects for TEM, CE, and thin film nano-fabrication applications.



(a) (b)

Figure 1: (a) Micrograph of a Cu via (targeted at 25 nm) x-section milled by 20 keV Ne+ beam at 1.5E+18 ions cm-2, (b) measured depth and width profile of 3 vias milled by 20 keV Ne+ beam in Cu with increasing dose. The target width for all three vias is at 25 nm. The via shown in (a) is represented by the blue line in (b).

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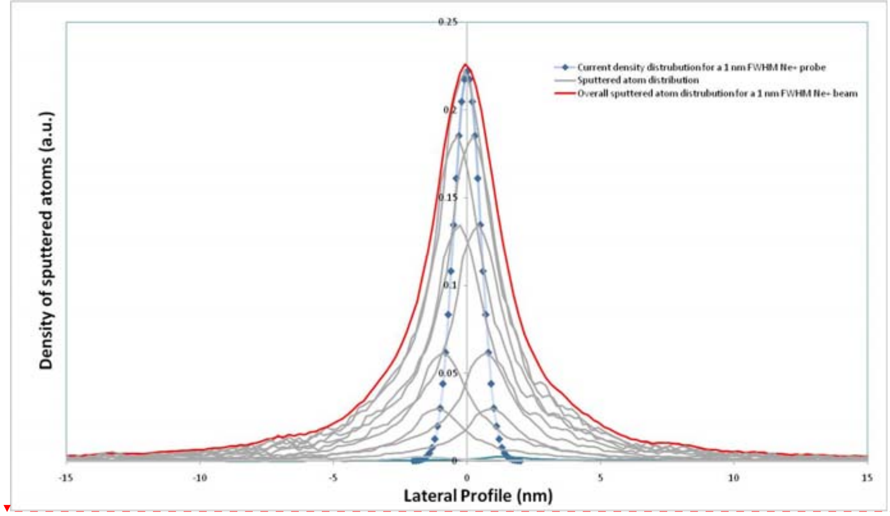

Figure 2: Simulation of sputtered copper atom lateral distribution by 20 keV Ne+ at 1pA with 1 nm FWHM. X axis represent the lateral location of the sputtered atom relative to the incident beam (X=0). Y axis represents the relative density of the sputtered atom at each lateral location. [7]

Reference

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