The Fabrication of Shallow Co-axial P-N Junctions on Silicon Micro/Nanopillars for Solar Cell Applications

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In this abstract, we detail the concept and process flow for fabricating vertical nanopillar solar cells with the core-shell and/or axial shallow *p-n* junctions formed using spin-on-dopant (SOD) solutions. Thin film (<50μm) and nanopillar based solar cells have been shown to be a desirable alternative to bulk solar cells since they can be fabricated on single crystal substrates and transfer printed on substrates that are inexpensive and often flexible.[1,2] The use of off-the-shelf commercial SODs in forming shallow junctions has not been extensively investigated and documented compared to its wide use in source-drain doping of MOSFETs on SOI[3].

We evaluated two different types of commercial SOD: Filmtronics P509 and Futurrex PDC1-2000. The experiment was initially conducted on planar silicon wafer test samples to provide a baseline process prior to optimizing the process for nanopillars. The two commonly used doping mechanisms of contact and proximity doping were carried out in a thermal furnace with a nitrogen atmosphere. In proximity doping, the SOD sample is positioned close to the device sample, while in contact doping, the SOD is coated directly on the device sample. Upon completion, the SOD is removed from the device by wet etching. Fig.1 shows an image of the undoped nanopillar samples. Spatial positioning of sample placement on the quartz boat placed in the tube furnace is shown Fig. 2. Both doping processes were done at 900^{o}C for equal amounts of time. Fig. 3 shows representative current-voltage (I-V) characteristics of a planar solar cell sample.

We show that shallow co-axial junctions can be created using SOD. Our fabrication method is low cost and could easily be adjusted to a high throughput process. By providing a low cost method to transfer devices from one substrate to another, our methodology offers a promising technique to create single crystal solar cells on flexible substrates such as plastic.

[1] A. Focsa et al., Heterojunction a-Si/poly-Si solar cells on mullite substrates, Thin Solid Films 516 2008 p. 6896-6901
[2] Hoon-Sik Kim et al., *Self-assembled nanodielectrics and silicon nanomembranes for voltage, flexible transistors, and logic gates on plastic substrates*, Applied Physics Letter **95,** 183504. 2004
[3] Z.T. Zhu et al., *Spin on dopants for high-performance single-crystal silicon transistors on flexible plastic substrates*, Applied Physics Letters **86,** 133507 2005

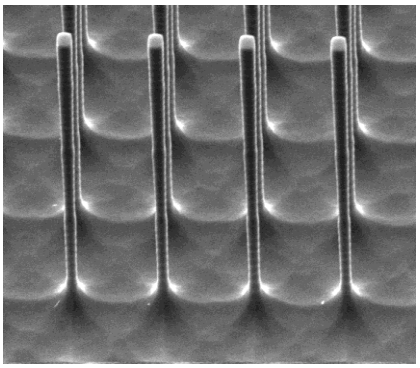

Figure 1. Si pillars DRIE etched for use as "Device Wafers" in the SOD project. These pillars can be then transferred onto a polymer (e.g. PMMA) coated low cost substrate.

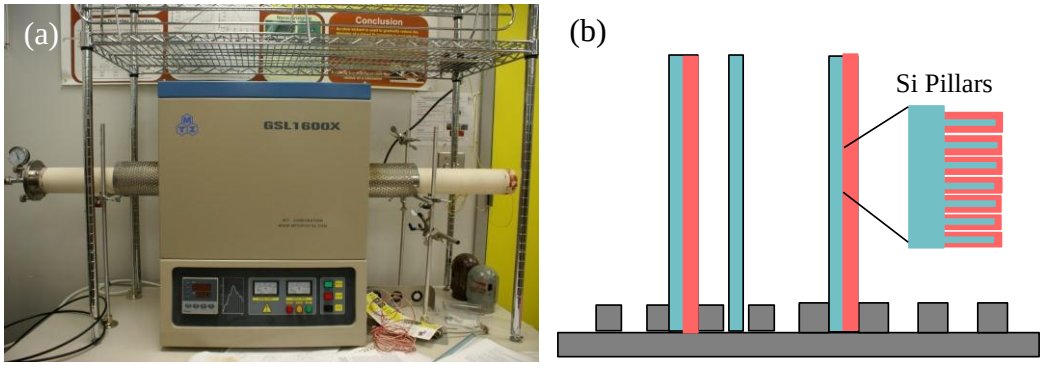

Figure 2. (a) Image of the tube furnace at UC Davis Inano lab and (b) schematic showing the spatial positioning of proximity (left) and contact (right) doping of silicon.

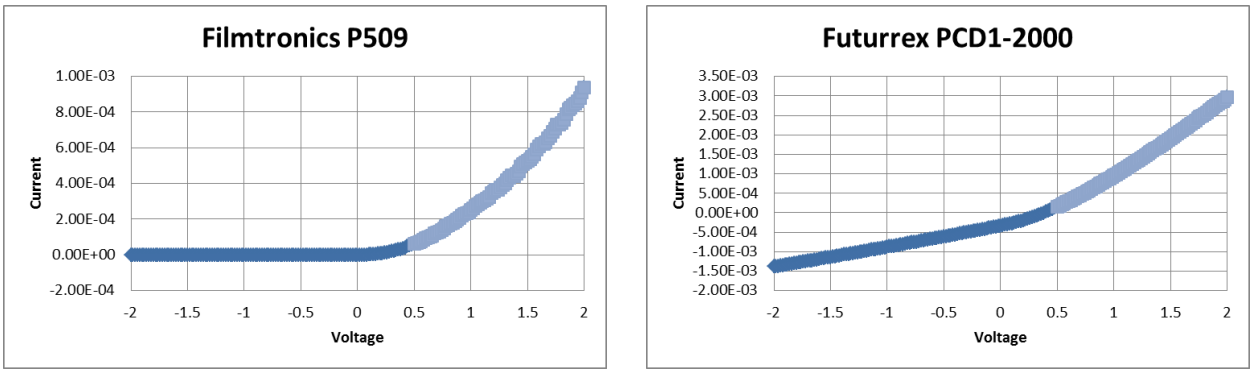

Figure 3. Current-voltage (I-V) characteristic of prototype planar solar cells. The representative performance of a sample doped using (left) Filmtronics P509 and (right) Futurrex PDC1-2000 is shown.