Monolithic 3D Integration

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3D-IC promises to offer multiple advantages over conventional 2D implementation, including alleviating the communication bottleneck, integration of heterogeneous materials, and enabling novel architectures. This paper will describe the monolithic 3D stacking of multiple active device layers optimized for Field-Programmable-Gate Array (FPGA) applications.

Recently, integration of nitrogen-doped AlO_x–based (AlO_xN_y) resistive change random-access-memory (RRAM) on CMOS was demonstrated [1]. They have been used as the configuration memory blocks in a 2- layer 3D-FPGA, which provides 1.6× improvement in tile density, 1.2× in speed and only 85% power consumption compared to conventional FPGA [2][3]. An improved architecture of 3-layer monolithic 3D FPGA with the insertion of a transistor layer promises further improvement in tile density, speed and power consumption [3].

To integrate another transistor layer on Si CMOS circuits, however, is challenging. All processes after CMOS must be kept below 400^{o}C. Several approaches have been proposed, such as epitaxial growth, chip bonding using through-silicon-via (TSV), and wafer bonding. It has been demonstrated that low temperature (<400^{o}C) wafer-scale Ge-to-SiO_2 fusion bonding with hydrogen-splitting is feasible [4]. Moreover, bonding of large Ge islands can improve the bonding yield and relieve the alignment precision requirement. The fabrication of Ge MOSFET on CMOS will be described. The integration of forming-free and sub-μA switching AlO_xN_y RRAM will be discussed. The functionality of 3D-FPGA will be demonstrated.

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