Invited Talk

Overcoming 3D-IC Technology Hurdles*

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Increasing the sensing and computational density within an integrated circuit can enable miniaturized intelligent subsystems that improve overall system data and energy efficiency. In a three-dimensionally integrated circuit (3D-IC), two or more layers of active components are combined such that signals pass between layers along a direct and shortened path length. For image sensors, such an architecture enables 100% fill factor pixel arrays with local image processing behind every pixel. For high-performance microprocessors or memories, 3D-IC has the potential to cut power consumption and increase data bandwidth significantly.

Lincoln Laboratory's approach to build 3D-ICs involves Silicon on Insulator (SOI) substrates, wafer-bonding and precision alignment of completed circuits, etching of deep, 1-micron diameter vias, and detector-layer thinning with smooth and uniform results. In Figure 1 we present a schematic illustration of a 3D-integrated image sensor that has per-pixel connections to a dedicated detector as well as to a local image processing circuit. Figure 2 shows an example SEM cross-section of a three-layer integrated circuit. The high aspect ratio 3D-Through Oxide Vias (3DTOV) are formed through silicon dioxide, and thus have lower parasitic capacitance than comparable TSVs[1]. We also applied both integrated-circuit level and package-level 3D integration to demonstrate four-side abuttable image sensor tiles[2], as shown in Figure 3. Finally in Figure 4 we show the results of heterogeneous integration of an InGaAs diode array with a SOI-CMOS readout circuit at a 6-micron pixel pitch[3].

In this talk we present lessons learned in methods, materials, and electrical characterization from several different applications of Lincoln Laboratory's 3D-IC technology. We discuss successes and challenges with 150-mm wafer based technology and project plans 200-mm wafer integration.

1. Burns et al., IEEE Trans. Electron Devices 53 (1): 2507-2516
2. Suntharalingam et al., Proc. ISSCC 09, 02.1
3. Chen et al., IEEE 3DIC2009, 28-30 Sept. 2009. pp. 1-4

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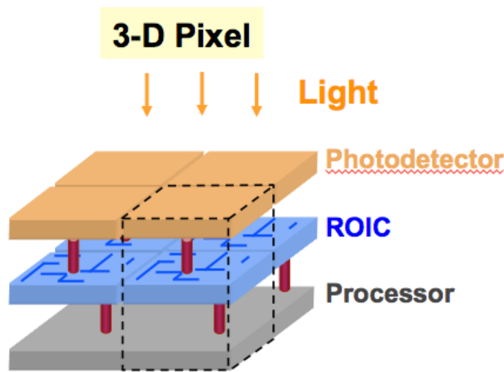

Figure 1: Illustration of a 3-D integrated pixel array that has 100% fill factor detectors and fabrication optimized by layer function.

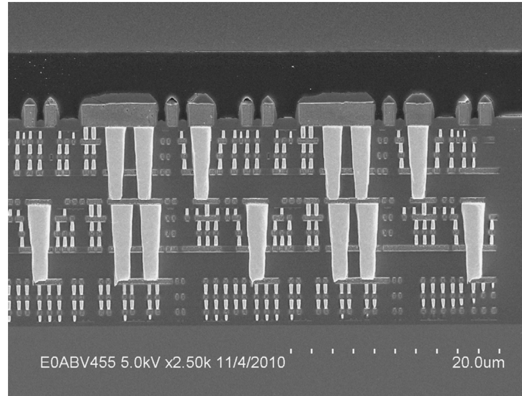

Figure 2: SEM cross-section of completed three-tier FDSOI CMOS circuit.

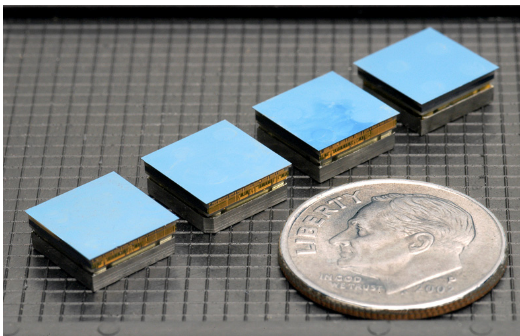

Figure 3: Photograph of four-side abutable image sensor tiles: 3-D integration is employed at both the integrated-circuit and package level to demonstrate a 1K x 1K CMOS active pixel sensor with high pixel fill factor, broad spectral response, and 64-channels of analog-to-digital conversion.

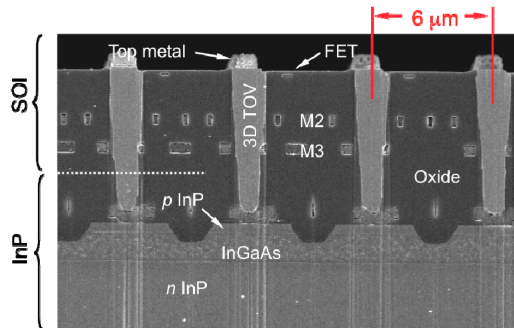

Figure 4: SEM cross section of two-tier circuit: The micrograph shows an array of 6-µm pitch vias connecting a InGaAs diode array to a SOI-CMOS readout circuit.