Heterogeneous 3D Integration

R.Patti
Tezzaron Semiconductor, Naperville. IL 60563
rpatti@tezzaron.com

Ever shrinking geometries have imposed further and further restrictions on the layouts that designers can create. These restrictions limit not only the actual geometric improvements, but also what the designers can implement. It is well known that analog circuitry does not scale well and indeed does scale at all in many circumstances. 3D integration offers an alternative to scaling that enables best of class processing to be applied to each circuit element.

To enable true 3D integration fine pitch Through Silicon Vias (TSVs) are required. A mistake often made is to view the required TSV pitch as being related to the total die area divided by the number of required connections. This approach however, is flawed. Just as the interconnect density requirement is not uniform across the die the TSV requirement is also not uniform. Indeed the TSVs tend to be required in the areas of highest congestion. Thus, larger TSVs with wide pitch become useless in addressing real 3D integration.

Tezzaron has assembled numerous 3D integrated circuits and demonstrated significant performance and power improvements. In this paper we discuss some of the homogeneous and heterogeneous devices that have been assembled and the resulting performance. TSV efforts from 120um pitch to 0.8um pitch are addressed and a discussion of their associated benefits and issues included.

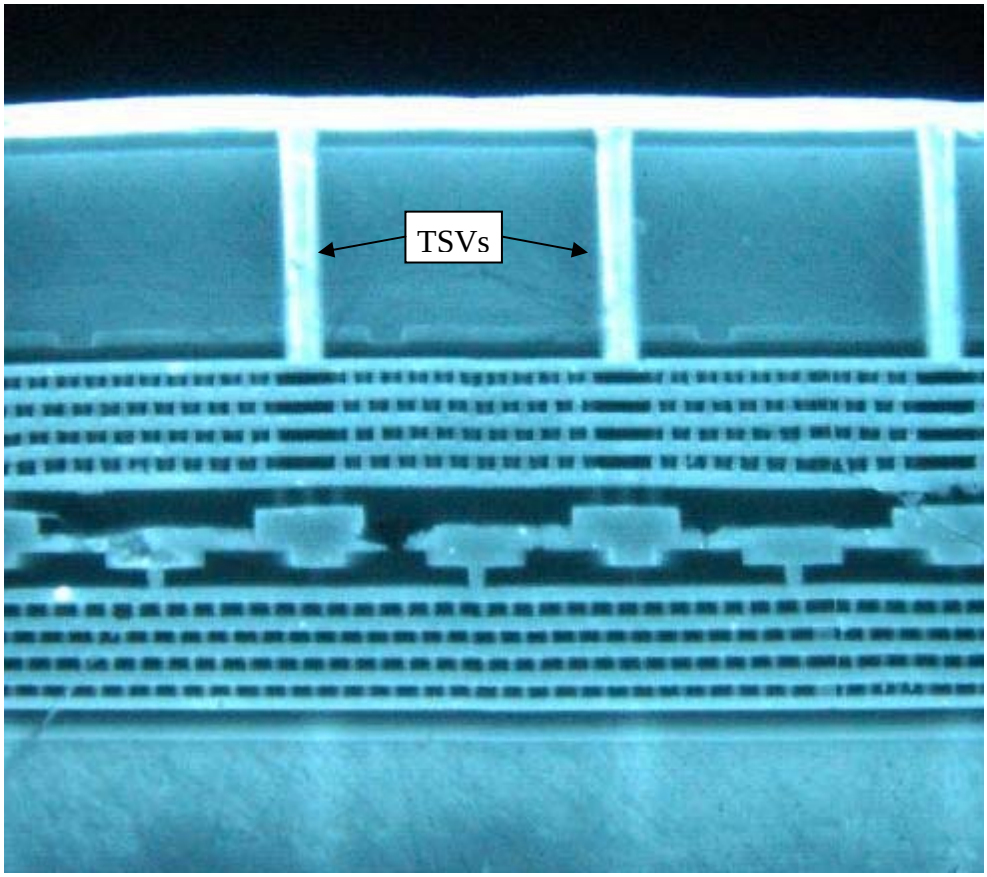

Figure 1: **SEM cut-away showing a 2 layer device stack with 5µm pitch TSVs**