An FPGA-based Pattern Generator for Massive Parallel High-Speed Nanolithography System

E. Ulin-Avila, L. Pan, S. Xiong, Y. Park, Y. Xiong, Y. Wang, C. Sun, D. Bogy, X. Zhang
Mechanical Engineering, University of California, Berkeley, CA 94720
xzhang@me.berkeley.edu

Optical lithography has been the standard technique allowing for the continuous reduction of device feature sizes in the semiconductor manufacturing process. However their resolution is fundamentally limited by light diffraction[1].Many alternative maskless approaches have been proposed[2-6] to further improve resolution but are limited by their serial and slow scanning nature. Plasmonic nanolithography (PNL)[7-8] offers deep subwavelength patterning resolution using a low-cost scheme that can satisfy high-throughput requirements by allowing massive parallel patterning at orders of magnitude higher scanning speed. However, this promising high throughput scheme also faces a great challenge for achieving required high overlay accuracy of subsequent layers which is strongly affected by inter-track stitching errors, consequence of the various time-delays existent in the system. Efficient time-delay handling and compensation is required to precisely synchronize the dynamics of the system with the independent addressing of multiple lenses.

Here, we use advanced clock domain control techniques for synchronous massive parallel pattern generation based on state of the art FPGA electronics. Our system truly synchronizes the triggering of electro-optic modulators to spindle CLK events and laser CLK events in order to compensate for angular positioning errors with ultrafine timing resolution. Finite State Machines (FSM) based on Look-up tables (LUTs) allow for independent, parallel task completion and adaptability to different user necessities, not only those of the PNL system. Hardware solutions for reduction of noise and disturbances on controlling signals are also detailed, such as, Digital Lock Loop (DLL) modules to reduce jittering of the various CLK domains. Achieved results support the feasibility and robustness of our approach. Compared to DSP-based control, this new scheme reduces time delay uncertainty from 20ns to 1.6ns, allowing the system (with 16,000 Lenses) to finish a 12 inch wafer in minutes. Additional ongoing changes in the system will be outlined to further improve the accuracy of this tool.

---

[1] S. Okazaki, J. Vac. Sci. Tech. B **9**, 2829 (1991).
[2] M. Muraki, S. Gotoh, J. Vac. Sci. Tech. B **18**, 3061 (2000).
[3] T. R. Groves, R. A. Kendall, J. Vac. Sci. Tech. B **16**, 3168 (1998).
[4] R. D. Piner, J. Zhu, F. Xu, S. H. Hong, & C. A. Mirkin, Science **283**, 661 (1999).
[5] R P. Vettiger, et. al., IBM J. Res. Develop. **44**, 323 (2000).
[6] K. Salaita, et. al., Chem. Int. Edn **45**, 7220 (2006).
[7] W. Srituravanich, et al. Nature Nanotech. **3**, 733 (2008).
[8] L. Pan. et al. Sci. Rep. **1**, 175 (2011).

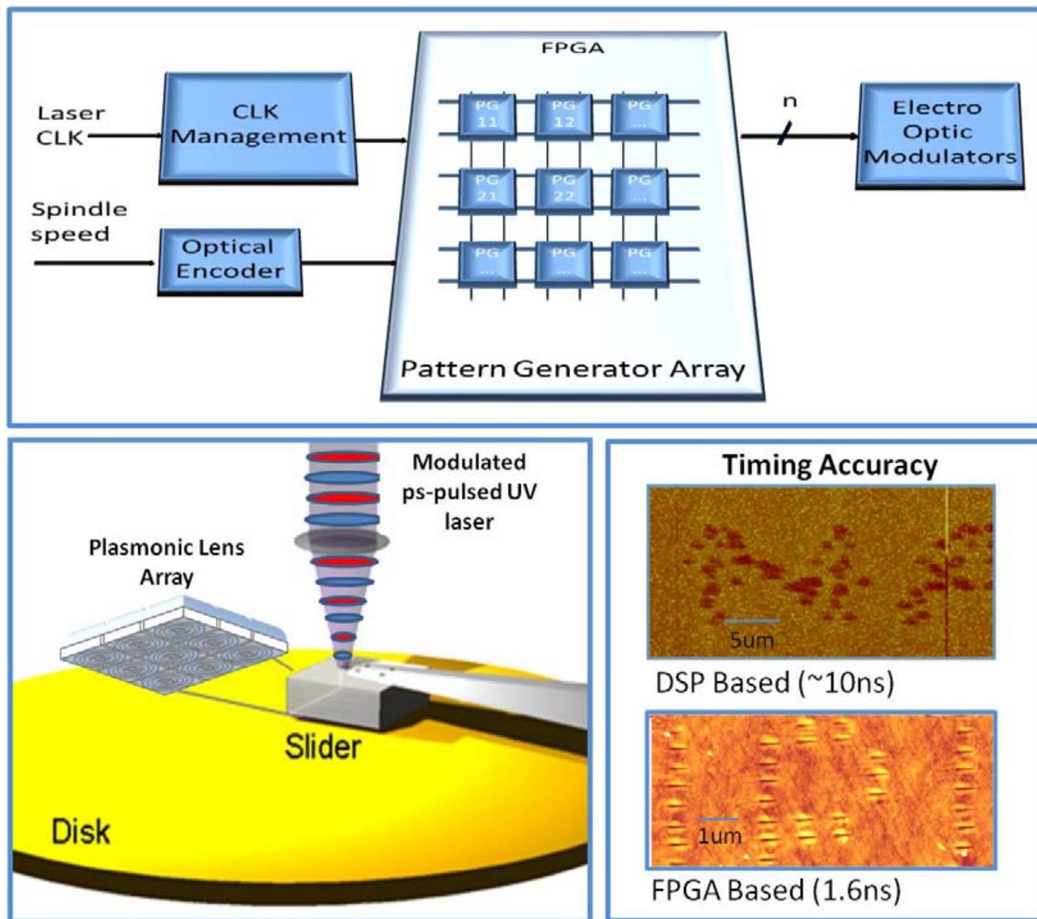

Figure 1: High-throughput scheme for Plasmonic Nanolithography: (Top) High-speed massive data transfer is achieved by implementing an array of pattern generators, synchronized by using CLK domain controlling techniques according to the dynamics of the PNL System (pico-second pulsed UV Laser source and Spindle). (Bottom left) Spaced by 3 um, thousands of plasmonic lenses can be independently addressed by individual optical beam and synchronized by advanced CLK domain controlling techniques allowed by FPGA reconfigurable electronics. (Bottom right) Results are compared to previously obtained results (DSP based)[7]. The patterned substrate with the word PIL shows the angular location reduced uncertainty improved by more than one order of magnitude after implemented our system.