# Nanofabrication of high aspect ratio (~50:1) sub-10 nm silicon nanowires using plasma etch technologies

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Si nanowires have a number of potential applications including healthcare sensors (especially for breath analysis), electrometers, quantum information processing devices, efficient thermoelectric generators and efficient Peltier coolers. Whilst the Bosch process[1] has been used to fabricate high-aspect-ratio anisotropic vertical Si structures, sidewall scalloping can causes a serious problem for producing vertical Si nanostructures. The Si etch process with $SF_6/O_2$ stimulated more interest once the cryogenic etch was developed[2], which can produce smooth sidewall through the enhancement of the sidewall passivation by the cryogenic cooling of the wafer. The low substrate temperature cryogenic process can create fabrication problems especially with resist, metal and passivation shrinkage, stress or cracking issues.

This paper addresses the challenges in achieving highly vertical Si structures with sub-10 nm resolution, smooth sidewalls and high aspect ratios at ambient temperature, which are crucial for many applications. In this work, we have developed simultaneous etch and passivation processes at 20 °C using an Oxford Instruments reactive ion etch (RIE) system with $CF_4/O_2$ plasma and a STS inductively coupled plasma (ICP) RIE system with $SF_6/C_4F_8$ plasma respectively. Both processes use thick HSQ resist as the etch masks. The final etch results of processes are critically determined by the simultaneous balance between etch and passivation during the plasma processing which can be achieved by optimizing the source and bias powers, gas flow rates, and chamber pressure. The results show that the ICP process with $SF_6/C_4F_8$ plasma is more suitable for deep Si etch duo to its low plasma induced damage, high etch rate and selectivity. Figures 1 and 2 show that reproducible highly vertical Si nanowire with sub-10 nm resolution, smooth sidewall and high aspect ratios up to ~50:1 have been successfully achieved at 20°C by using the STS ICP tool with $SF_6/C_4F_8$ plasma under the optimized etch conditions. The HSQ lines with widths of 5, 10, 20 and 30 nm were patterned by the VB6 UHR e-beam lithography tool with resist thickness of 150 and 250 nm which provides the flexibility of direct pattern transfer with very high resolution. Therefore, we expect that the developed plasma etch process combined with an optimized HSQ mask will provide more reliable technologies for device fabrications of less than 10 nm.

[1] J.K. Bhardwaj, H. Ashraf, Proc. SPIE Micromachining and Microfabrication Process Technology 2639, 224–233 (1995).
[2] S. Tachi, K. Tsujimoto, and S. Okudaira, Appl. Phys. Lett. **52**, 616 (1988).

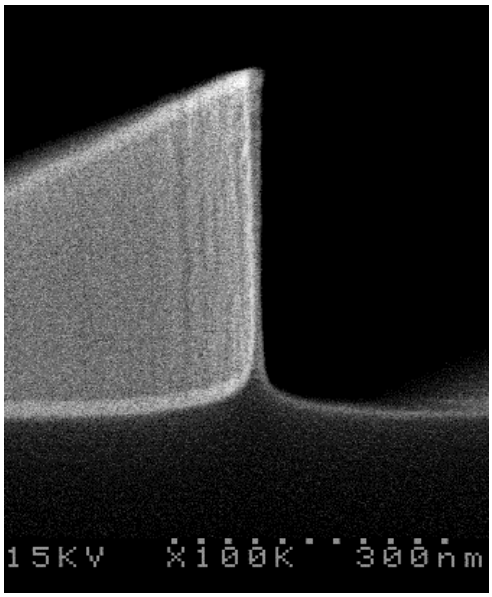


Figure 1: The SEM image taken by Hitachi S-900 SEM without any metal coatings shows the cross section of a vertical Si nanowire with sub-10 nm width, ~350 nm high, and aspect ratio ~35:1. The HSQ resist mask is still left on the top of the Si nanowire, which was etched by a STS ICP tool with a $SF_6/C_4F_8$ plasma.

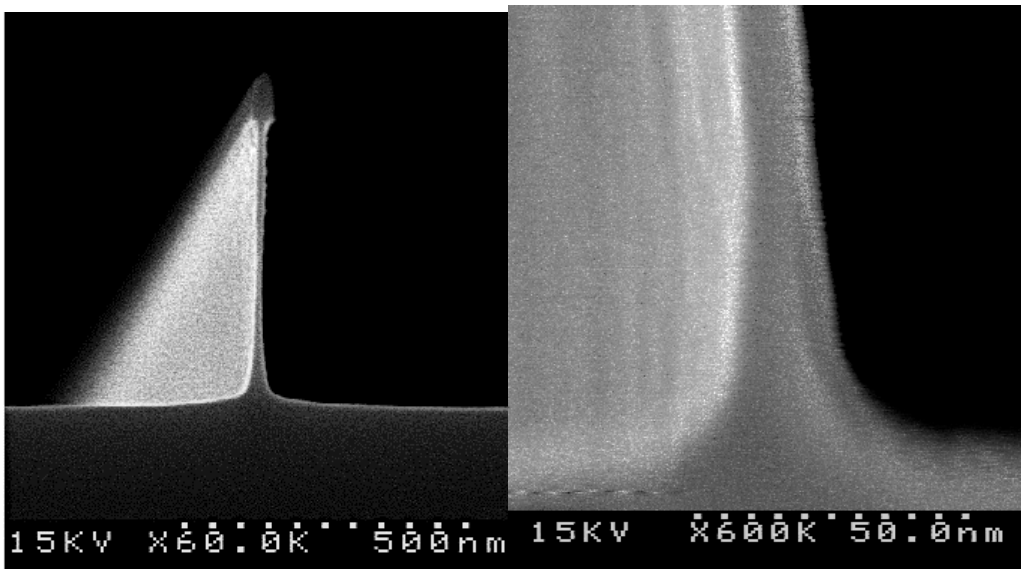


Figure 2: The SEM image taken by Hitachi S-900 SEM without any metal coatings shows the cross section of a highly vertical Si wire with sub-10 nm width, 500 nm high and aspect ratio ~ 50:1. The HSQ resist mask is still left on the top of the Si nanowire, which was etched by the ICP with $SF_6/C_4F_8$ plasma.