Electron beam lithography-based grating customization strategies for gate level patterning in high density SRAM circuits

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CMOS density scaling relies on a decrease in the contacted gate pitch (CGP) for each new technology node. As CGP has dropped below 150 nm the use of double exposure, double etch (DE^2) techniques to create gate patterns has become common practice[2]. DE^2 improves pattern fidelity by deconvolving the gate pattern into a 1D grating-like pattern and a 2D customization pattern (fig. 1 a-c) allowing each exposure to be optimized independently. DE^2 also creates the opportunity to choose a different lithography method for each of the two exposures. Electron beam lithography (EBL) has demonstrated the resolution and overlay accuracy required for use in a grating customization application. Progress in EBL tool design may result in an improvement in throughput to a level appropriate for development or low volume production[3,4]. However, the integration of EBL with a DE^2 process for circuit patterning is largely unexplored.

In this work, we investigate EBL as a technique for grating customization of gate level patterns in SRAM circuits based on the FinFET device architecture. We explore both gate first and replacement metal gate (RMG) process flows. For gate first processing, a grating pattern is transferred into a SiN layer aligned to the underlying fin pattern (figure 2). EBL is performed in a positive tone resist to form the space between adjacent gate ends. This image is transferred into the SiN layer followed by transfer of the composite pattern into the gate stack. For RMG processing, the gate pattern remains as a 1D grating pattern through the dummy gate encapsulation and removal process (figure 3). EBL with Hydrogen Silsesquioxane (HSQ) resist is used to form the dielectric regions between adjacent gate ends. This results in the formation of discrete gates after gate stack deposition and planarization. An extension of the gate first process to a circuit with 50 nm CGP is shown in Figure 4 (b). The use of DE^2 with EBL shows a significant improvement in pattern fidelity. Results from functioning CMOS inverter circuits from both processes are shown in figure 4 (c-d). The results demonstrate that EBL can achieve the overlay required to customize pre-existing grating patterns. Moreover, EBL creates unique process integration opportunities that may ultimately simplify circuit fabrication. This work was sponsored by the DARPA GRATE (Gratings of Regular Arrays and Trim Exposures) program under Air Force Research Laboratory (AFRL) contract FA8650-10-C-7038.

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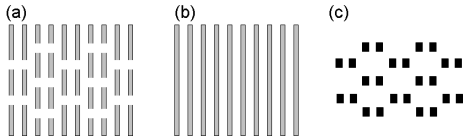

Figure 1: example of gate level pattern decomposition for an SRAM circuit using the DE^2 approach showing: (a) the complete 2D gate pattern (b) a 1D grating pattern containing the gate pitch and critical dimension information of the pattern and (c) a 2D pattern containing the gate line end position and end-to-end spacing information.

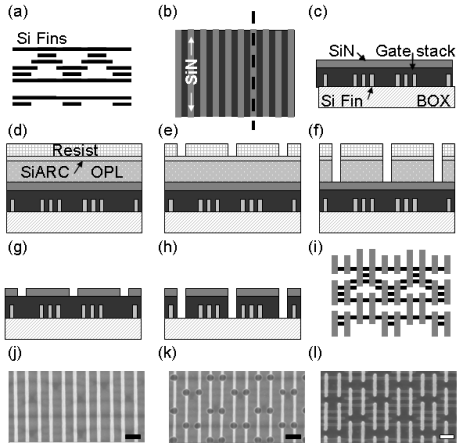

Figure 2: Process for customizing gratings for gate level patterns in a gate first FinFET process flow. (a) Si fins are patterned on a buried oxide layer (BOX) to define active regions of the transistors. (b) A gate stack consisting of a high-κ dielectric, a work function setting metal, amorphous Si and SiN is deposited onto the substrates. Lithography and RIE are used to define a grating like pattern in the SiN hardmask. (c) A cross section through the structure corresponding to the dashed line in (b). (d) A positive tone resist is applied to a layer of Si containing anti-reflective coating (SiARC) and an organic planarizing layer (OPL). (e) EBL is used to pattern the location of spaces between gate ends. (f) The pattern is transferred into the SiARC and OPL stack using RIE. (g) Pattern transfer into the SiN followed by removal of the remaining OPL. (h) final RIE into the gate stack materials. (i) plan view of the final structure (j) shows an SEM image of the initial structure after RIE of the grating pattern into the SiN. (k) and (l) show SEM images of steps (g) and (h) respectively. The scale bars in (j-k) correspond to 100 nm

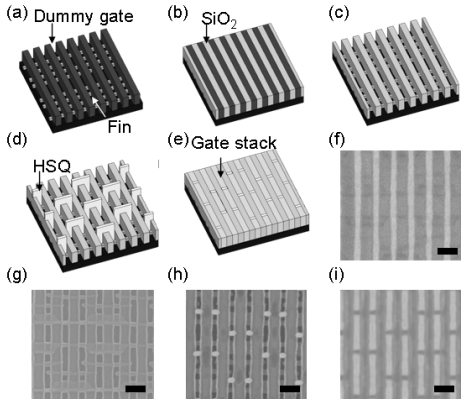

Figure 3: Process for customizing gratings for gate level patterns in a RMG FinFET process flow. (a) Amorphous Si dummy gates are patterned over Si fins using conventional lithography and RIE. (b) The dummy gates are encapsulated in SiO_2. The SiO_2 layer is planarized using chemical mechanical polishing (CMP) revealing the dummy gates. (c) The dummy gates are removed selective to the SiO_2 and Si fins. (d) EBL is performed using HSQ as a resist to directly form the dielectric regions between adjacent gate ends. (e) Gate stack deposition and planarization is performed using a combination of atomic layer and chemical vapor deposition techniques followed by CMP. (f-i) SEM images of the process steps shown in (b-e). The scale bar in the SEM images corresponds to 100 nm.

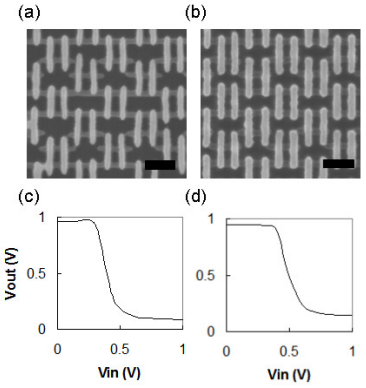

Figure 4: single level patterning (a) compared to DE^2 patterning with EBL customization (b) for an SRAM circuit fabricated using gate first processing feature a 50 nm CGP. The scale bar in both images corresponds to 100 nm. CMOS inverter curves for circuits fabricated using DE^2 with EBL customization in gate first (c) and gate last (d) process flows featuring a 90 nm CGP.