Sub-20nm Hybrid Lithography enabled by Highly Regular Layout, Pitch Division, and e-Beam Exposure

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Semiconductor patterning is facing a crisis as 2007 marked the last year in which a higher λ/NA optical scanner was introduced. For advanced sub-20nm CMOS technology nodes, no single approach to patterning will be suitable for high volume manufacturing.[1] However, a hybrid approach appears to be feasible. A path to 7nm CMOS using hybrid patterning has been described, with some issues noted for nodes beyond 16nm.[2]

The hybrid concept combines four existing technologies: circuits designed with highly regular layout, optical lithography for "lines" at pitches of >80nm, spacer-based pitch division, and e-beam-based lithography for "cuts" and holes. This approach using optical lithography, self-aligned patterning, and e-beam lithography has been referred to as CEBL – "Complementary e-beam Lithography."

Conventional logic design has used 2D patterns with bends and other non-rectangular shapes. A different design style, using highly regular 1D gridded features, has been developed to enable effective use of a "lines" and "cuts" division of the patterning problem.[3,4] Figure 1 shows a comparison between 2D conventional and 1D gridded design styles.

Once "line" patterns have been formed with optical lithography, pitch division using a self-aligned spacer approach will be required.[5] Figure 2 shows where pitch division by 2 and by 4 will be required for Metal-1 line patterning.

To complete the circuit patterning, e-beam lithography will be needed for the "cut" and "hole" exposure. For high volume manufacturing, multiple column e-beam systems will be required for throughput while maintaining placement accuracy.

An example metal-1 pattern using lines and optical cuts is shown in Figure 3 for 22nm design rules with a 70nm pitch. The simulated optical cut pattern is merged with the lines to show the expected results after patterning. The SEM image shows the Damascene trenches in photoresist. (Photo courtesy of Applied Materials.)

A serious problem for 1D gridded design of SOCs (System on Chip) is the current approach of designing logic cells and SRAMs with different styles. For example, typical SRAMs have the gate and metal-1 lines parallel, while the standard cells have these layers in perpendicular directions. The alternative is to design the logic and SRAMs to be unified from the beginning. In this case, critical layer orientations as well as pitches can be matched.[6]

Figure 4a and 4b show example layouts of logic cells and SRAM arrays, respectively. The gates are all aligned, on the same pitch. The metal-1 pattern, not shown, runs horizontally in both layouts, also on the same pitch. This unified design approach is required to support a 1D gridded design style implemented with lines and cuts.

Implications of CEBL for SOC designs will be discussed. The limitations of optical lithography for the cut and hole patterns will be presented, along with a discussion of current efforts in direct write e-beam lithography with emphasis on multiple beam approaches.

Keywords: gridded design rules, highly regular layout, CEBL, multiple e-beam lithography, spacer double patterning

REFERENCES

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FIGURES

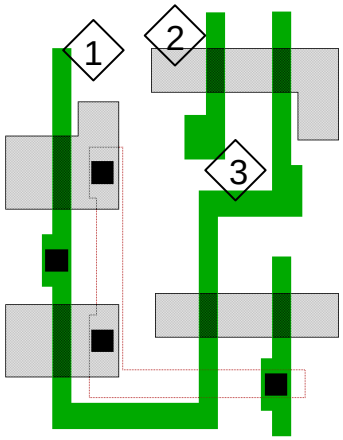

Figure 1a. Conventional 2D logic design style with problem areas: 1) isolated line, 2) semi-isolated line, 3) 2D bends and corners.

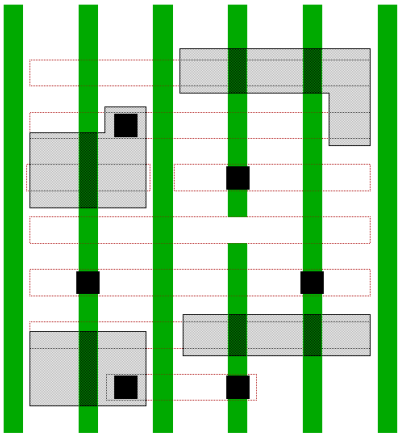

Figure 1b. 1D gridded design for CMOS logic.

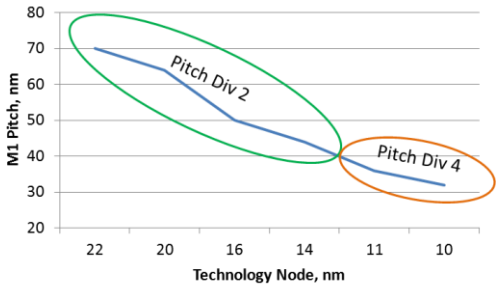

Figure 2. Metal-1 pitch trend for CMOS logic, with pitch division by 2 and 4.

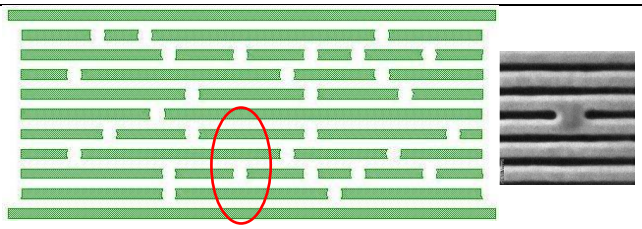

Figure 3. Metal-1 pattern with simulated optical cut pattern and SEM of Damascene trenches.

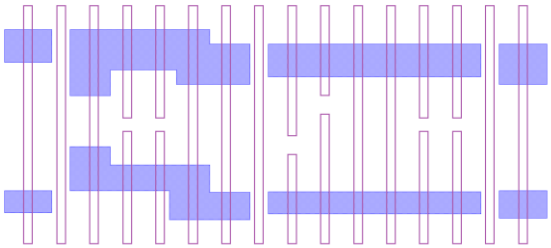

Fig.4a. Standard cell Active and Gate layers.

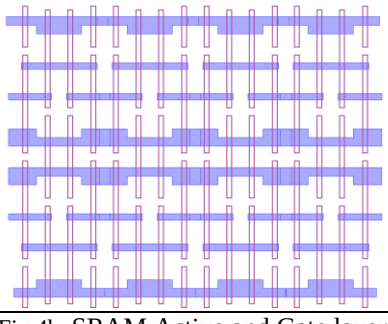

Fig.4b. SRAM Active and Gate layers.