Capped carbon hard mask an innovative route to nanoscale device fabrication

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The capability to fabricate sub-20 nm nanostructures is now essential to develop new NEMS, electronic or biologic devices. So far, it has been demonstrated that some lithographic techniques like nanoimprint [1], e-beam [2] or EUV [3] can potentially achieve sub-20 nm structures. Nevertheless, they are not currently suitable for industry applications due to high defect density, cost, exposure time or resist problems. Other techniques like spacer patterning [4], resist trimming [5, 6] allow to reduce pattern resolution but in that case the process flow is rather complex.

In this study, we demonstrate the possibility to obtain sub-10nm patterns on 8-inch wafers by using materials which can be easily implemented on a device process flow without dramatically increasing the fabrication cost. For this purpose, we have used a bilayer stack composed of an amorphous carbon hard mask capped by a thin silicon oxide layer of about 20nm (Fig. 1). This technique consists first in transferring resist patterns into the oxide layer, then in opening the hard mask [7]. The carbon hard mask subsequently undergoes an anisotropic trim in order to reduce the initial resist pattern dimensions [8, 9] (Fig. 1 and 2-B), and transfer is finally carried out into the stack which is to be patterned (Fig. 3).

The main advantage of using a capping layer is to reduce critical dimensions (CD) while preserving the initial pattern height: hence, the pattern aspect ratio is increased. Furthermore, in such configuration the role of resist patterns is limited to etching the thin oxide capping layer, which considerably reduces resist budget (approximately the thickness of the capping layer here) and contributes to suppress resist thickness limitations.

In the presented example, resist patterns were performed by hybrid lithography (e-beam/deep UV) with a negative chemically amplified resist. E-beam exposures were carried out on a Leica VB6UHR 100KV from Vistec, optical lithography on a KrF ASML stepper (248 nm). The initial resist dimensions were 30 nm (Fig. 2-A). After carbon hard mask trimming optimisation (Fig. 2-B), 7 nm polysilicon/TiN gates were obtained (Fig. 3), which is a state-of-the-art result for a “low cost” patterning process.

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[1] Chou et al., J. Vac. Sci. Technol. B 15.6., Nov/Dec 1997
[2] A.E. Grigorescu et al. / Microelectronic Engineering 84 (2007) 822–824
[3] B. Pivanranta et al., Nanotechnology 22 (2011) 375302
[4] K.-H. Chung, Jpn. J. Appl. Phys. Vol. 41 (2002) pp. 4410–4414, Part 1, No. 6B, June 2002
[5] M. Ono, M. Saito, and T. Yoshitomi, J. Vac. Sci. Technol. B 13, 1740 (1995)
[6] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B26(6), p2583 Nov/Dec 2008
[7] Y. X. Liu et al., IEEE Int. SOI Conf. 2005, p. 219
[8] S. Pauliac-Vaujour et al. / Microelectronic Engineering 85 (2008) 800–804
[9] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B 25, 2030 (2007)

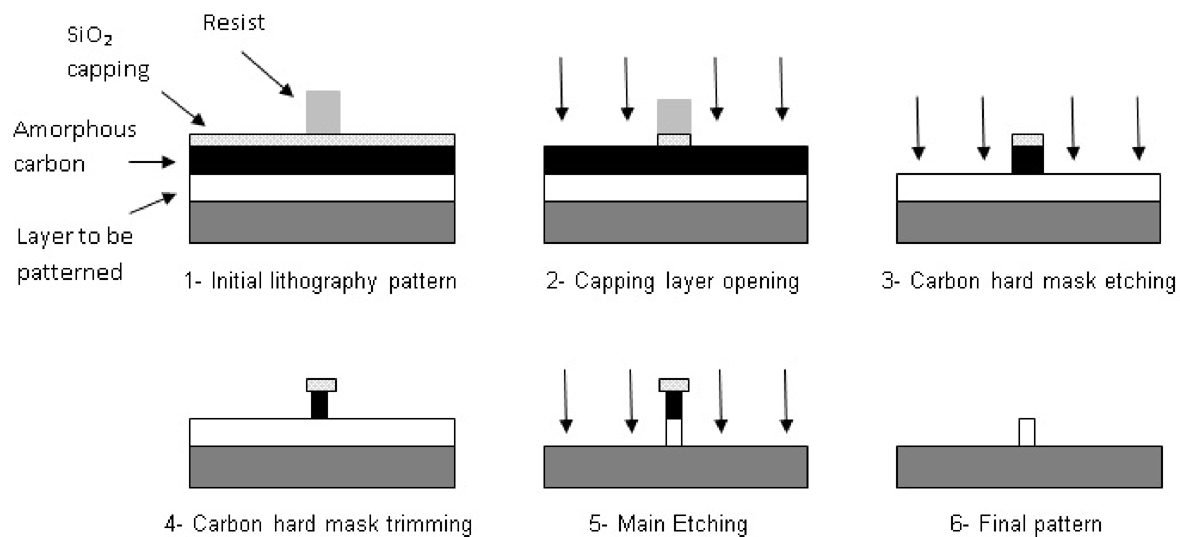

Fig. 1: Process flow by using a capped carbon hard mask

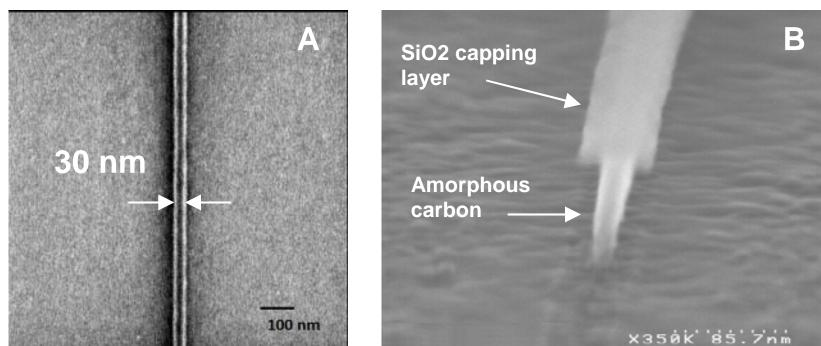

Fig. 2: Top SEM view of initial resist patterns (A) and Cross sectional SEM view of capped amorphous carbon pattern (B)

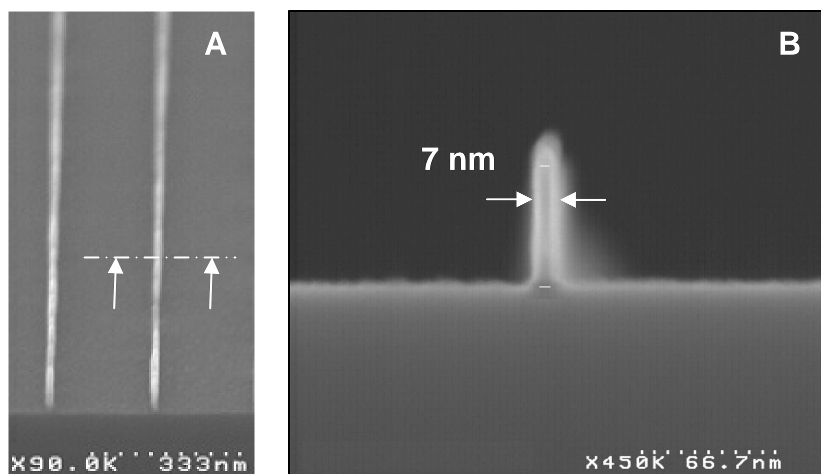

Fig. 3: Tilted (A) and Cross sectional (B) SEM views of 7 nm transistor gates