Horizontal Growth of Silicon Nanowire Arrays for Large-Scale Circuit Applications

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Semiconductor nanowires are among the promising candidates for future electronics. However, most of the nanowire devices and circuits have been made from randomly positioned wires and are not suitable for large-scale integration, which requires precise control of the position and orientation of each nanowire. Meanwhile, horizontal nanowires are preferred because of the simplicity in making electrical contacts. However, previous efforts [1-5] resulted in horizontal nanowires at random positions and out-of-plane growth.

Here we present a nanowire growth method that simultaneously meets three requirements: horizontal growth, controlled position and orientation, and growth on an insulator. The first step is to prepare the substrate. We fabricated 80nm-thick Si sidewalls with (111) orientation (Fig.1A) using potassium hydroxide (KOH) wet etch on a silicon-on-insulator wafer with the top Si layer having a (110) orientation. An HF etch into the buried oxide created a gap of 70 nm between the bottom of the Si (111) sidewall and silicon dioxide floor and will allow nanowires to grow horizontally without touching the floor.

The critical and challenging step is to place gold catalyst dots precisely on the sidewalls without undesirable gold on the top of Si or on the SiO_2 floor. We patterned strip arrays in PMMA that are orthogonal to the sidewalls using electron beam lithography (EBL). Then, the gold was evaporated with an 80° tilt so the thickness of gold films on the sidewalls is much larger than those on Si top and on SiO_2 floor (Fig.1B). After potassium iodide (KI) wet etch with precise time control, the gold on Si top and SiO_2 bottom were removed while the gold dot arrays on the sidewalls remained (Fig. 2). The size of gold dot is determined by sidewall thickness, EBL stripe width, gold film thickness and KI etching time.

Silicon nanowires were grown in a chemical vapor deposition reactor using $SiCl_4$ as precursor with Boron doping at 850°C and 1 atm. The successful growth of horizontal Si nanowire array is shown in Fig. 3. Fixing the suspended horizontal nanowires for subsequent device fabrication processes was achieved by atomic-layer deposition of 50 nm Al_2O_3, which fills the gaps between the nanowires and the SiO_2 floor. Device and circuit fabrication is on-going and will be reported.

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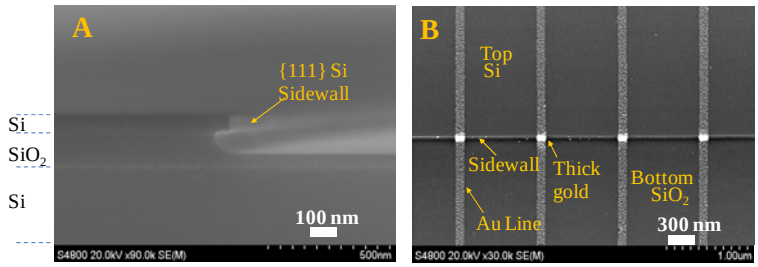

Figure.1 (A) Cross-sectional view of the substrate. (B) Top view of the substrate after deposition of gold strip array.

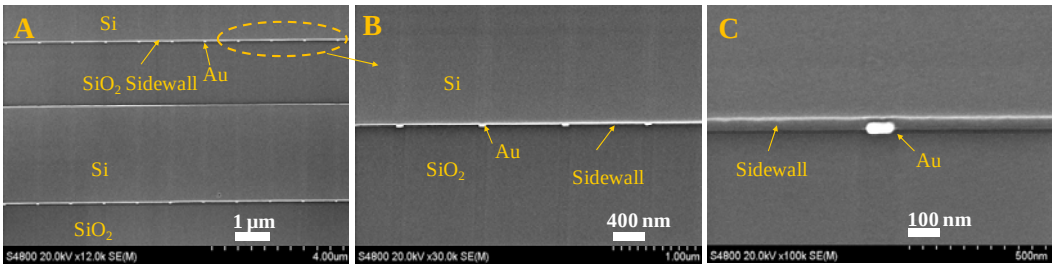

Figure.2 (A), (B), (C) SEM images of gold dot arrays on {111} sidewall: (A) and (B) are top views. (C) was taken with a 30° tilt.

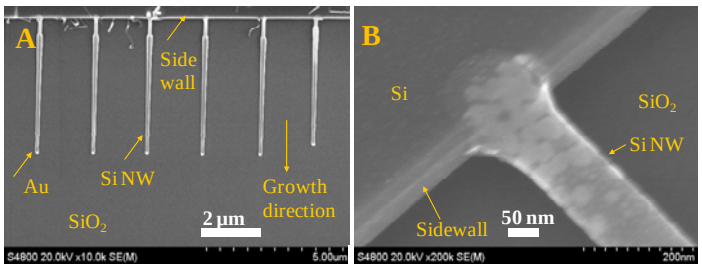

Figure.3 (A) Top view of horizontal nanowire array. (B) Zoom in of the "root" of a nanowire at the sidewall. SEM micrograph was taken with a 30° tilt.