Directed Self-Assembly for the Semiconductor Industry

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Abstract

The semiconductor industry will qualify and ship 22 nm technology node VLSI circuits starting in 2012 [1]. The continued scaling of feature size has brought increasingly significant challenges to conventional optical lithography [2-4]. The rising cost and limited resolution of current lithography technologies have opened up opportunities for alternative patterning approaches. Among the emerging patterning approaches, block copolymer self-assembly for device fabrication has been envisioned for over a decade. Previous research by the groups of Hawker, Russell, and Nealey [2-4] has shown a high degree of dimensional control of the self-assembled features over large areas with long range ordering and periodic structures. The exquisite dimensional control at nanometer-scale feature sizes is one of the most attractive properties of block copolymer self-assembly. At the same time, device and circuit fabrication for the semiconductor industry requires accurate placement of desired features at irregular positions on the chip. For 22 nm technology node and beyond, the required 3-sigma value of lithography for critical dimension (CD) control and overlay (registration of one layer to another layer of lithography) accuracy for microprocessors are below 2.3 nm and 8.0 nm (3-sigma values), and the parallel line pitch is below 80 nm [5]. The need to coax the self-assembled features into circuit layout friendly location is a roadblock for introducing self-assembly into semiconductor manufacturing. Directed self-assembly (DSA) and the use of topography to direct the self-assembly (graphoepitaxy) have shown great potential in overcoming the current lithography limits [4,6]. In this paper, we review recent progress in using block copolymer directed self-assembly for patterning sub-20 nm contact holes for practical circuits.

Recognizing that typical circuit layouts do *not* require long range order, we adopt a lithography sub-division approach akin to double-patterning and spacer patterning, using small guiding topographical templates. Guiding topographical templates with sizes of the order of the natural pitch of the block copolymer can effectively guide the self-assembly of block polymer. Therefore, circuit contact hole patterns can be placed at arbitrary location by first patterning a coarse guiding template using conventional lithography [7-8] (Fig. 2). The strong lateral confinement from the small topographical template sidewall changes the natural (often hexagonal for cylindrical domains) arrangements of the block copolymer [7] (Fig. 1). This procedure enables generating a higher resolution feature at a location determined by the coarse lithographic pattern. The size and

registration of the features are determined by parameters of the template as well as the block copolymer itself. Preliminary analysis of the size and positional accuracy of small template DSA shows great promise [8] (Fig. 3).

Pattern transfer of the block copolymer soft mask into device layers is necessary for device fabrication. Using conventional reactive ion etching, DSA contact hole patterns are transferred to dielectric layers and subsequently filled with metals that make electrical contact to the devices [10] (Fig. 4). Transistors and simple circuits such as inverters have been demonstrated using block copolymer DSA for contact hole patterning [10] (Fig. 5).

The first demonstration of using this small template DSA approach for industry standard circuits is the contact hole patterning for 22nm SRAM [8]. 193-nm immersion lithography is used to print the templates for 22-nm node 6T-SRAM cells reported by IBM [9]. The contact for the polysilicon-to-diffusion cross-over of the SRAM cell is implemented by a two-hole contact pattern (Fig. 2c) instead of an elliptical contact in the original design (Fig. 6). Well-formed 25nm contact hole patterns with overlay accuracy around 1nm are obtained (Fig. 7) by block copolymer DSA [8].

Furthermore, the contact holes for more complex random logic circuits patterned by this small template DSA approach has also been demonstrated for selected standard cells in an open-source standard cell library adapted for 22-nm node CMOS (Fig. 8) [11]. For the first time a DSA-aware design methodology for a gridded design rule-based (GDR) layout is developed. The contact holes were achieved with a critical dimension (CD) of 15 nm and overlay accuracy around 1 nm using guiding templates with a CD of 51 nm. It is also shown that DSA is able to heal the template defects.

Besides the flexible control of DSA, defectivity has always been one of the main concerns for DSA commercialization for semiconductor manufacturing. The defectivity of PS-b-PMMA block copolymer following a typical graphoepitaxy contact hole rectification process (Fig. 2a) on a 300mm wafer flow is studied. The missing via defectivity rate using this DSA hole-shrink technique has recently been reported to be less than 1-per-25-million vias [12]. This result reinforces the commercializability of this patterning technique.

Acknowledgement

This work is supported in part by the Keck Foundation, the NSF (CMMI 1029452) and Global Research Collaboration (GRC) of the Semiconductor Research Corporation (SRC). Collaborations with Prof. Subhasish Mitra and Dr. Jie Zhang at Stanford University are gratefully acknowledged.

Supplement

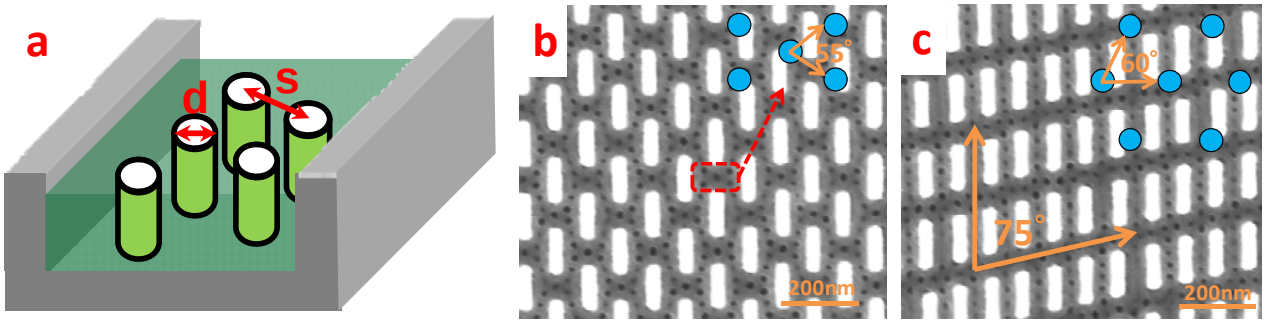

Fig. 1. (a) Graphoepitaxy with self-assembled cylinders aligned in the trench center. d represents the diameter of the cylinder and s represents the nearest center to center distance. (b) – (c) Self-assembled holes on pre-patterned templates with dimensional scales close to its nature size / pitch. The physical confinement forces the self-assembly to rearrange according to the array of the templates thus breaking the inherent hexagonal closed pack structure. Inset of (b) shows the included angle between two neighboring holes is 55°. Inset of (c) shows the hexagonal closed pack with an included angle of 60° while the templates in (c) drives the angle between neighboring holes to 75°. After Chang *et al*. [10].

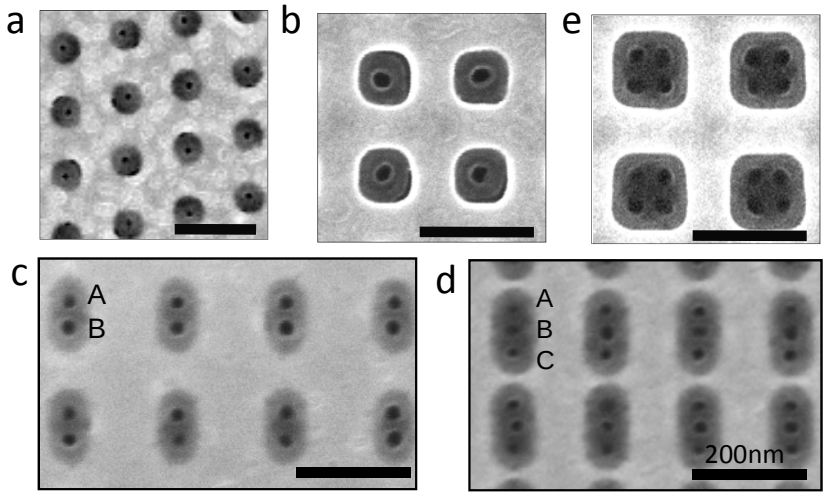

Fig. 2. SEM images of DSA patterns confined by small templates. Templates are patterned using conventional optical lithography and etched into 50 nm depths. Single hole in (a) 75 nm and (b) 92 nm square templates. (c) 4-hole square lattice patterns in 126 nm square templates. (d) 2-hole patterns in 60 nm × 110 nm rectangle templates. (e) 3-hole pattern in 70 nm ×145 nm rectangle templates. Scale bar 200 nm. After Bao *et al*. [8].

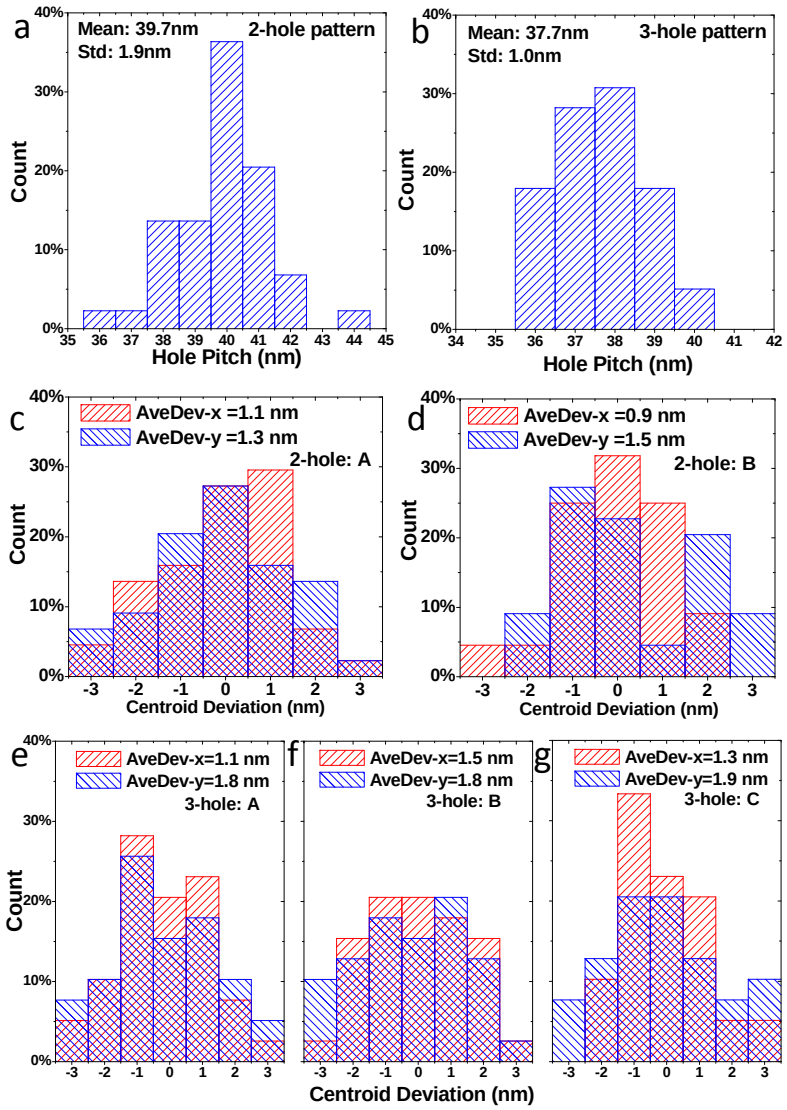

Fig. 3. The pitch analysis for (a) two-hole pattern in Fig. 2d and (b) three-hole pattern in Fig. 2e. (c) and (d) Overlay accuracy of two-hole pattern. The average absolute deviation (AveDev) in x and y direction is 1.1 nm and 1.3 nm (upper row hole A), 0.9 nm and 1.5 nm (lower row hole B), respectively. Overlay accuracy of three-hole pattern. (e) Upper hole A. (f) Middle hole B. (g) Lower hole C. The AveDev for all the DSA patterns is less than 2 nm, indicating a good position registration accuracy and repeatability. After Bao *et al*. [8].

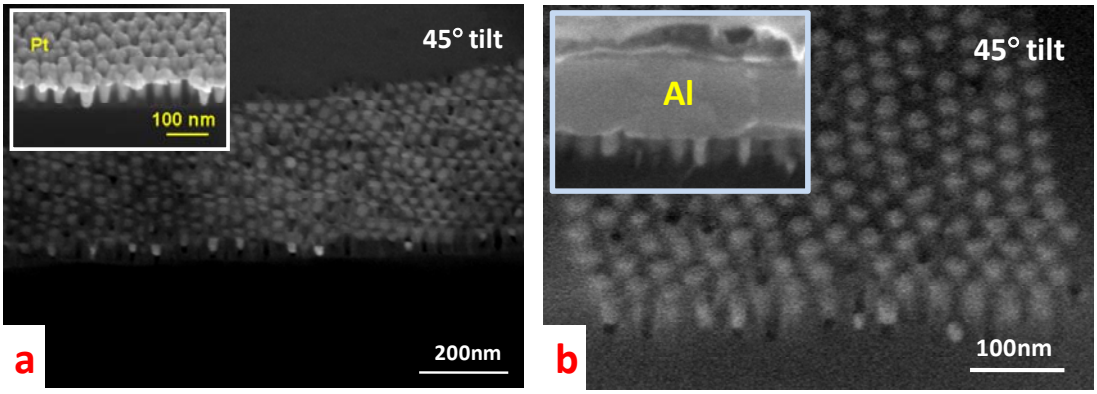

Fig. 4. SEM micrographs showing self-assembled 18nm contact holes in lithographically pre-defined trenches after pattern transfer from PS-PMMA template to inter-layer-dielectric by reactive ion etch. The contact holes are then filled with metals (a) Pt by atomic layer deposition, followed by Al deposition (b) to form electrical contacts. After Chang *et al.* [10].

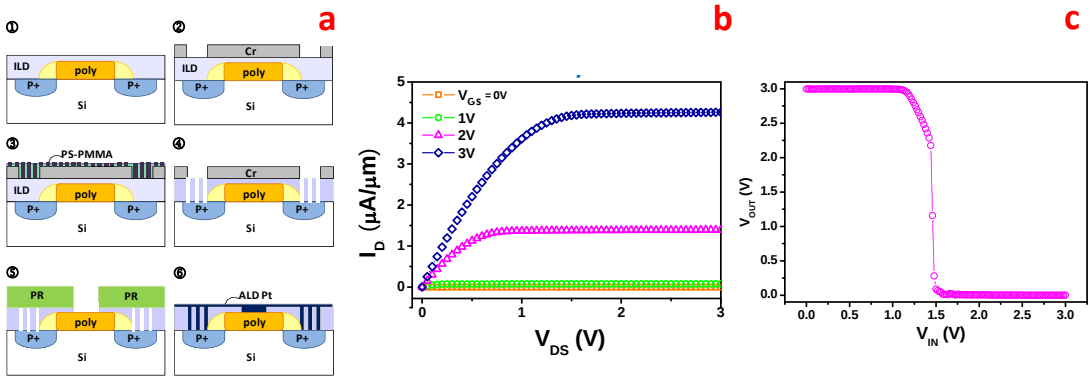

Fig. 5. (a) Process flow for fabricating self-assembled contact holes for contacting the source/drain of a top-gated MOSFET. (b) *I-V* characteristics of the fabricated nFET with nanometer-sized Pt contact holes. The V_T (V_{DS} = -100mV) extracted using the peak gm method is ~0.8V. (c) Transfer curve of fabricated CMOS inverter with 20nm contact holes. V_{DD}=3V. After Chang *et al.* [10].

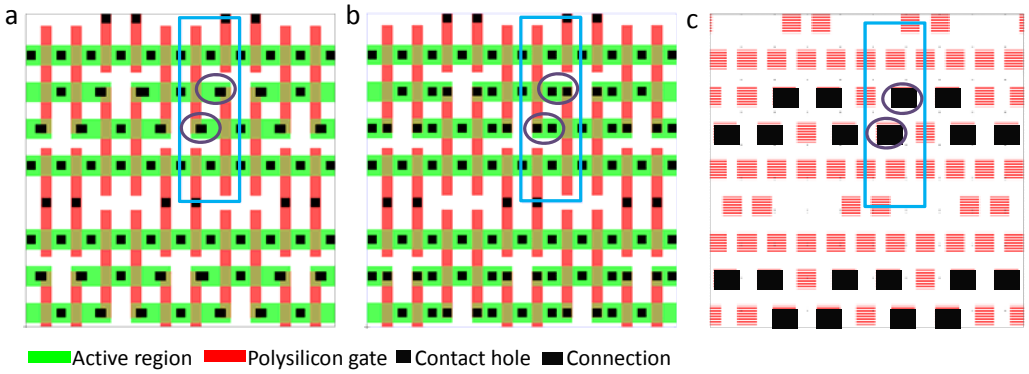

Fig. 6. (a) Contact hole layout derived directly from the IBM 22-nm 6T-SRAM [7]. A unit cell is outlined by a blue rectangle (dimension 180 × 554 nm^2). (b) Modified layout by replacing the rectangular connections with hole-pairs (highlighted by purple ellipses). One hole contacts the active region and the other hole contacts the polysilicon gate. (c) Immersion 193 nm optical lithography mask design for guiding templates of SRAM contact holes. Black rectangles are designed for the two-hole patterns as connections between the polysilicon gate and the active diffusions. After Bao *et al*. [6].

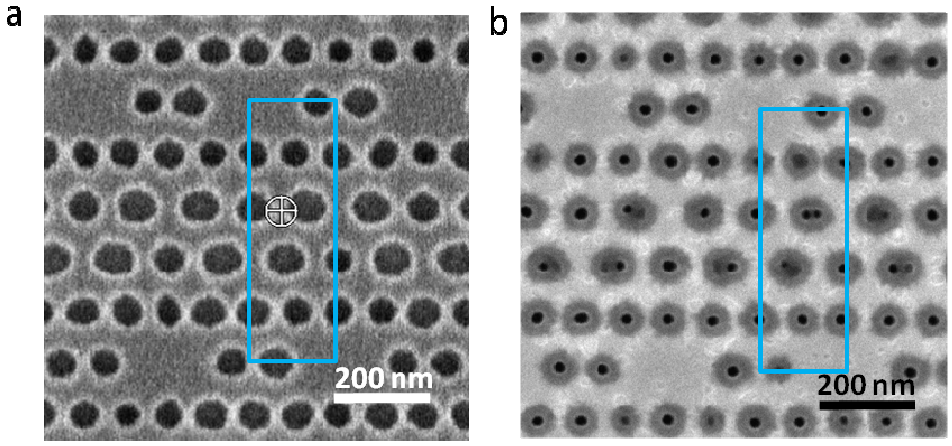

Fig. 7. (a) SEM image of the guiding templates for SRAM, fabricated by 193 nm immersion optical lithography and conventional etching process. (b) DSA patterns in the fabricated guiding templates after removing the PMMA blocks. Single holes are generated inside square templates and hole-pairs are generated in rectangular templates, as designed in Fig. 4. The unit SRAM cell is outlined by blue rectangles. The very few blurred holes in the pattern are possibly a result of electron beam damage during SEM imaging. After Bao *et al*. [6].

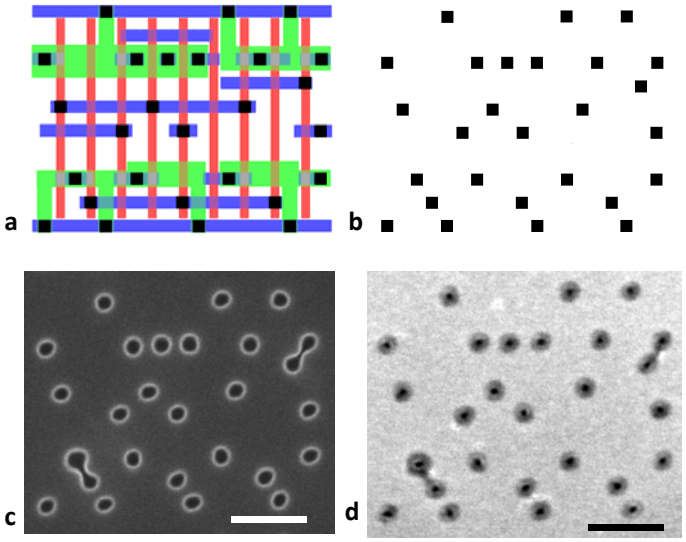

Fig. 8. (a) DSA-aware HA-X1 (half adder) layout. (b) Contact layout. (c) SEM image of half adder guiding template, after etching. Some templates are connected due to proximity effects of e-beam exposure (see Fig. 9 also). (d) DSA patterns in the guiding templates. Note that the DSA holes that appear inside the connected templates are separate, showing the healing of defects of the guiding template. Scale bar: 200 nm. After Yi *et al*. [11].

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