Via-Hole Fabrication for III-V Triple-Junction Solar Cells

Yuning Zhao, Patrick Fay
Department of Electrical Engineering, University of Notre Dame, 275 Fitzpatrick Hall, Notre Dame, IN 46556
pfay@nd.edu

Andree Wibowo, Jianhong Liu, Chris Youtsey
MicroLink Devices, Inc. 6457 W. Howard St. Niles, IL 60714

Backside contact technology is a promising method for increasing solar cell performance significantly by reducing optical shadowing by placing all electrical contacts on the back of the solar cell [1,2]. A new contact technology is under development for InGaP/GaAs/InGaAs inverted metamorphic (IMM) triple junction solar cells for epitaxial-liftoff cells (see Fig. 1). A key process for realizing backside-contact triple junction solar cells is via-hole fabrication, as these provide the interconnection from the top-side GaAs emitter cap layer to the bottom of the cell (see Fig. 2 for the heterostructure). To fabricate the via-holes, all of the epitaxial layers, which consist of multiple layers of mixed III-V materials approximately 13 μm thick in total, are etched through; strongly anisotropic etch profiles are necessary for minimizing the area lost to the vias. To date, there have been very few reports of processes suitable for implementing these structures in solar cells.

In this work we demonstrate a three-step etching process for via-hole fabrication. The etching process includes two steps of Cl_2/Ar inductively coupled plasma reactive ion etching (ICP RIE) [3,4,5] followed by a simple highly-selective wet etch [6,7]. Both trench and via patterns were used to investigate the etching process. A SiO_2 etch mask (deposited by PECVD) was used; the III-V samples were mounted on Si carrier wafers with thermal grease and etched in an Oerlikon Shuttleline ICP-RIE. Helium backside cooling was used during etching to control sample temperature.

Fig. 3 shows a SEM image after 10-minute high temperature (180 °C) Cl_2/Ar ICP RIE. Anisotropic etch profiles were obtained and the selectivity to the SiO_2 mask was larger than 13. The concave-shaped bottom of the etch, however, is potentially problematic. To eliminate this feature a lower temperature (50 °C) Cl_2/Ar ICP-RIE step was employed to flatten the bottom and etch into the InGaP junction. Fig. 4 shows a typical SEM after this step, demonstrating the flat bottom and near vertical sidewalls. Finally, a selective wet etch ($HCl:H_3PO_4 = 2:1$) was used to etch through the InGaP junction and stop at the GaAs emitter cap layer without sidewall undercutting[8], as shown in Fig. 5. This wet etch also reduces any plasma damage in the contact area. The developed process produces nearly vertical, uniform, and smooth sidewalls despite the complex heterostructure and compositional variations, as needed for via interconnects in advanced solar cells.

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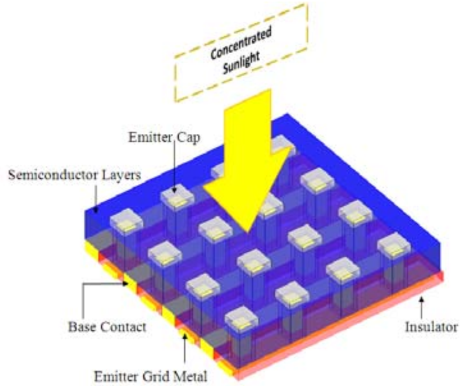

Figure. 1: Overview of epitaxial-liftoff backside-contact triple junction solar cell structure.

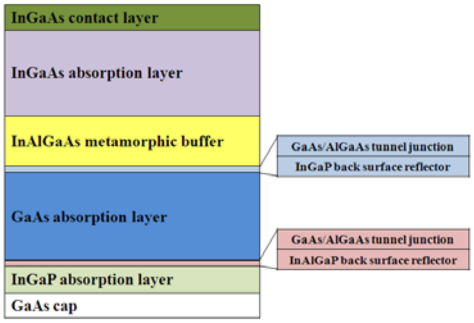

Figure 2: Cross-sectional cartoon of the triple-junction solar cell heterostructure. The overall epitaxial layer thickness for etching the vias is approximately 13 µm.

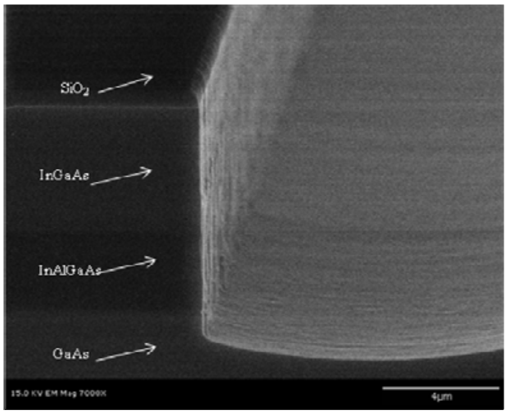

Figure 3: Typical SEM micrograph of the triple-junction solar cell etched at 180 °C for 10 minutes. The etching conditions were: 5 sccm Cl_2*, 10 sccm Ar, 100 W RIE power, 300 W ICP power, 2 mTorr and 180 °C.*

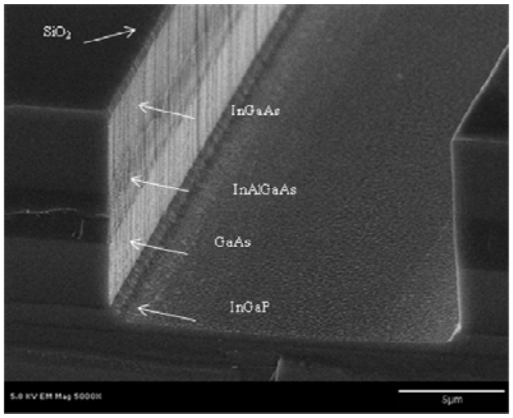

Figure 4: SEM micrograph of the triple-junction solar cell after two-step etching, which included a 180 °C ICP RIE followed by a 50 °C ICP RIE. The etching conditions of the 50 °C ICP RIE were: 12 sccm Cl_2*, 3 sccm Ar, 100W RIE power, 300 W ICP power, 2 mTorr and 50 °C*

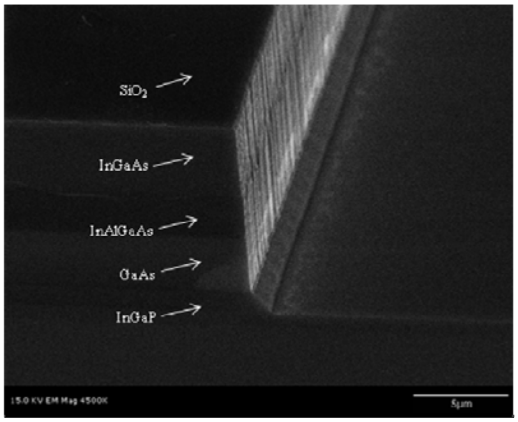

Figure 5: SEM micrograph of the triple-junction solar cell after wet etching.