CMOS Compatible RF MEMS Technology

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A monolithically integrated RF CMOS-MEMS capacitor technology is now in production at IBM's 200mm semiconductor fabrication facility in Burlington, Vermont. MEMS capacitors are being fabricated using a 0.18μm generation high voltage 50V-LDMOS/5V-CMOS technology with the MEMS formed with the final three refractory metal cladded AlCu wiring levels in SiO_2 [1]. MEMS cavities are formed using a novel planar sacrificial silicon process derived from IBM's damascene copper contact switch MEMS process [2] and are hermetically sealed at wafer level with a CVD dielectric lid.

Figs. 1 and 2 show the MEMS beam structure with a metal/oxide/metal sandwich beam and the lower capacitor electrode under the beam. The MEMS cavity, beam, and lid are integrated above the CMOS and 5 levels of BEOL AlCu and Cu wiring. A planar silicon lower (LC) and upper (UC) cavity process is used to form a cavity around the MEMS beam and the silicon is vented through holes in the oxide lid (V) using XeF_2 gas, which releases the MEMS beam. The cavity is then sealed by depositing CVD SiO_2 and Si_3N_4 to provide a hermetic seal. This planar cavity process reduces both MEMS beam fatigue during switching and also dissipates stress on the lid during chip packaging.

Maintaining capability with CMOS fabricator manufacturing equipment was a critical requirement in the development of this RF MEMS technology. The process has been implemented and L1 qualified using conventional materials including Silicon, Ti, TiN, AlCu, SiO_2 and Si_3N_4. CMOS capability has enabled rapid introduction in a stable, high volume production facility. This CMOS compatible RF MEMs technology is now in early production providing chips for antenna tuning in cell phones.

1. A Stamper, C. Jahnes, S. Dupuis, A. Gupta, Z.-X. He, R. Herrin, S. Luce, J. Maling, D. Miga, W. Murphy, E. White, S. Cunningham, D. DeReus, I. Vitomirov, and A. Morris, in Proc. 16th Transducers,Beijing,China,June 5-9,2011, pp.1803-6.
2. C. Jahnes, N. Hoivik, J. Cotte, M. Lu, and J. Magerlein, in Proc. Solid State Sensors, Actuators, and Microsystems Workshop, Hilton Head Island, SC, United States, June 4-8, 2006 pp. 360-3.

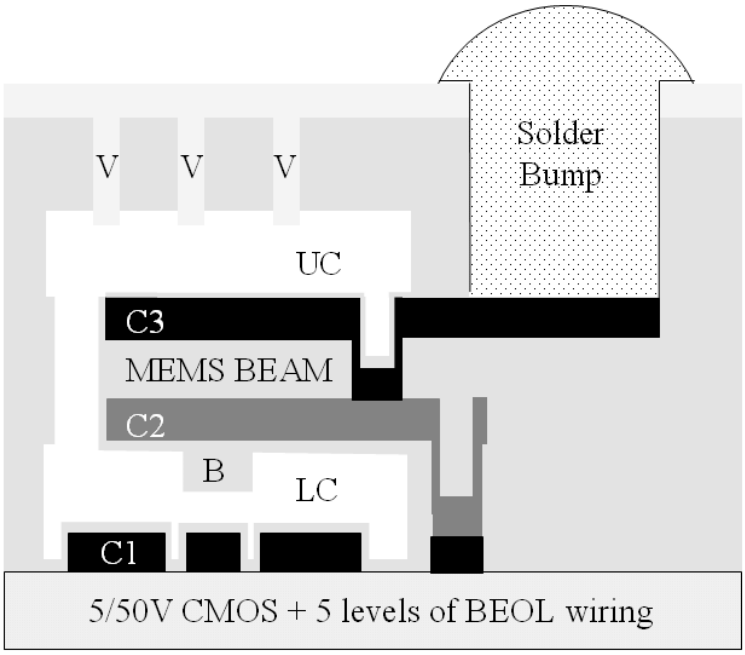

Figure 1: Simplified cross-sectional drawing of 0.18μm generation 200mm wafer planar MEMS technology.

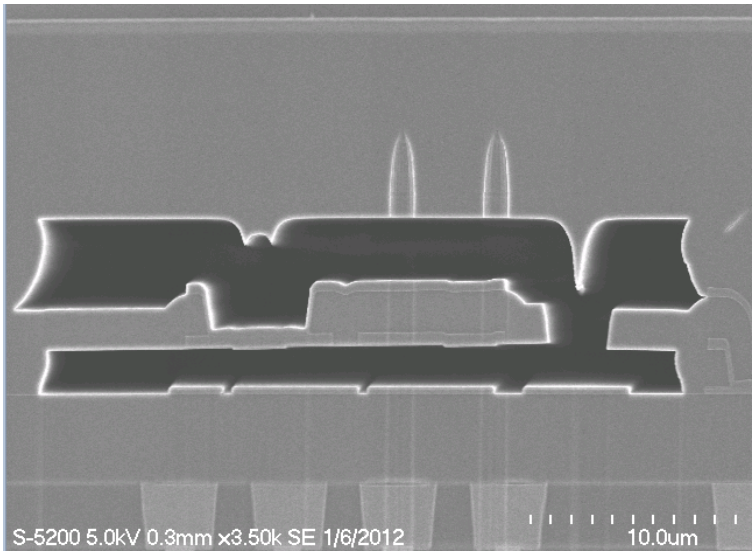

Figure 2: SEM cross-section of released MEMs beam test structure