Sub-30 nm pitch circuit relevant patterning in Si, SiO_2 and SiN using directed self assembly-based pattern generation

Hsin-Yu Tsai*, Sebastian Engelmann, Hiroyuki Miyazoe, Michael Guillorn
IBM Watson Research Center, 1101 Kitchawan Road, Yorktown, NY 10598, USA

Chi-Chun Liu, and Joy Cheng
IBM Almaden Research Center, 650 Harry Road, San Jose, CA 95120, USA

Line-space pattern generation using directed self-assembly (DSA) of block copolymers (BCPs) combines lamellae forming self-assembling materials with lithographically defined template patterns to produce a grating-like pattern [1]. DSA was shown to result in frequency multiplication of template patterns printed at pitches obtainable by 193 nm immersion (193i) lithography [2]. This results in the generation of patterns with a sublithographic resolution determined by the composition of the BCP [2-4]. Consequently, this technique could be used to extend the application of single exposure 193i lithography to sub 30 nm pitch patterning. C. Bencher et al. reported the first results obtained from a wafer-scale DSA patterning process demonstrating low defectivity after selective removal of one of the BCP domains and transfer into poly-Si [5]. In this work, we present a systematic study of the DSA pattern generation process. Etch process parameters and their impact on pattern fidelity are presented for 3 target materials: Si on insulator (SOI), SiO_2 and SiN. Demonstration of templating and pattern transfer for circuit relevant patterning is also presented.

Fig. 1 shows the process integration used in this work. Results for pattern transfer into SOI, SiN, and TEOS-based SiO_2 are shown in Fig. 2. A BCP consisting of poly(styrene-block-methyl methacrylate, PS-b-PMMA) was used to generate "fingerprint" patterns on full 200mm-wafers. Our results shows that a moderate ion energy is required to maintain etch selectivity of PMMA over PS [6]. A reduction in the plasma density achieved by significant reduction of the input power was required to improve the process window for both selective PMMA removal and the hardmask etch. These changes in plasma process conditions reduced pattern distortion of the PS/PMMA features, a phenomenon commonly observed when patterning lines in the sub 80 nm pitch regime. [7] After the hardmask etch, the pattern was transferred into the underlying organic planarization layer (OPL) using an O_2-based plasma chemistry. Further pattern transfer into the underlying material was carried out using appropriate processes for each material (Fig 2-b). Use of a graphoepitaxy-based template scheme allowed the formation of discrete numbers of self-assembled lines registered to pre-existing patterns (Fig. 3). This enabled a quantitative study of the top-down line edge roughness (LER) and line width roughness (LWR) evolution during various stages of the pattern transfer process. Results obtained for pattern transfer into SiN are shown in Fig. 4 for 1, 2 and 10 discrete DSA lines. The data shows that while LER remains roughly constant, LWR is reduced during the pattern transfer process. Measurements of pattern placement of the DSA lines relative to the template patterns indicate placement error on the order of the measured LER for 1, 2 and 10 DSA lines. This work is sponsored by the DARPA GRATE (Gratings of Regular Arrays and Trim Exposures) program under Air Force Research Laboratory (AFRL) contract FA8650-10-C-7038.

* htsai@us.ibm.com

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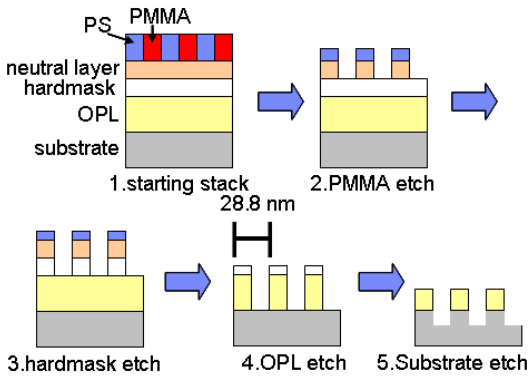

Figure 1: Film stack and etch process integration. A multilayer consisting of an organic planarizing layer (OPL) and a deposited SiOx hardmask are used to extend the etch budget of the DSA pattern.

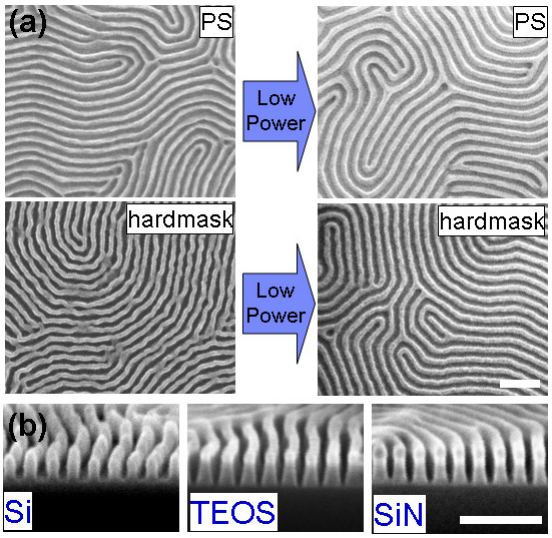

Figure 2: (a) Pattern fidelity improvement of BCP and hardmask etch achieved by reducing the plasma power. Eliminating pattern distortion during the hardmask etch was critical for reducing LER and LWR. (b) Etch transfer into 20nm SOI, 40nm silicon nitride, and 40nm TEOS with fingerprint patterns from a 28.8nm-pitch PS-b-PMMA polymer. The scale bars shown in (a) and (b) correspond to 100 nm.

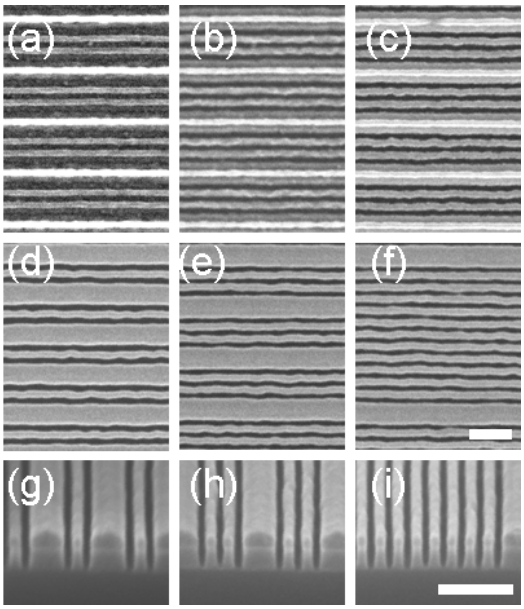

Figure 3: Pattern transfer of templated BCP lines showing results after PMMA removal (a), hardmask etch (b), OPL etch (c) and final etch into a 40 nm-thick SiN film (d). The ability to form 1, 2 and 10 discrete lines is demonstrated in (d), (e) and (f) respectively. Profiles of (d) – (f) are shown in (g) – (i) prior to removal of the OPL from the SiN film. The scale bar for (a)-(f) and (g) – (i) correspond to 100 nm.

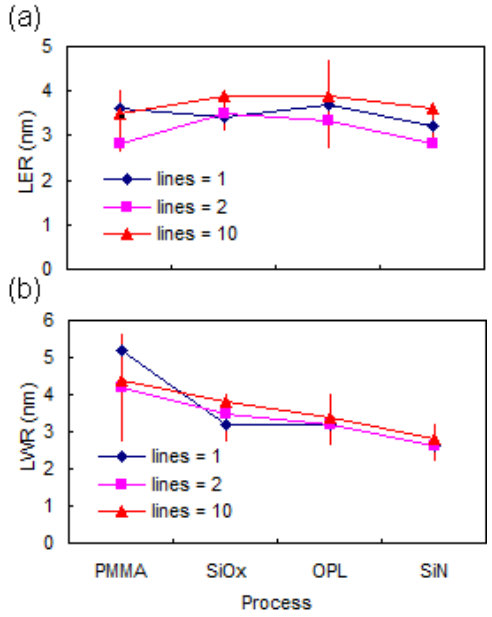

Figure 3 Quantitative study of the top-down LER and LWR evolution through the various stages of the pattern transfer process for SiN patterning.