Fabrication of On-Chip Fluidic Ion Channels using Self-Aligned Double Layer Resist Processing Technique

Bongho Kim[1], Jihun Kwon[1], Daehong Kim[1], Sungwoo Chun[1], Hyungyu Lee[1]
Seonjun Choi[1] and Seung-Beck Lee[1,2,3*]

[1]Department of Electronic Engineering, Hanyang University, Seoul, Korea
[2] Institute of Nano Science and Technology, Hanyang University, Seoul, Korea
Fax: +82-(0)2-2294-1676, Tel: +82-(02)-2220-1676, E-mail address:
sbl22@hanyang.ac.kr

The design and fabrication of artificial ion channels has received great attention since it may contribute to the development of on-chip ionic potential transport channels and also lead to applications in biomolecule sensors. Nowadays, several corresponding artificial ion channels have been designed, most of which were based on trans-membrane proteins, peptide or non-peptide molecules in lipid bilayers [1].

Here, we report on a new method to fabricate on-chip fluidic channels with electrostatically controllable nano-valves acting as ion channels. We have fabricated 10 nm diameter nano-valves using a self-aligned double layer resist patterning process. The on-chip fluidic channel dimensions are formed in the 800 nm thick poly(methylmethacrylate) (PMMA) positive electron-beam resist (PER) and then AR-N 7520 (2-methoxy-1- methylethylacetate) negative ER (NER) was spin coated on top of the patterned PMMA (Fig.1(a)). The 50 nm NER pillars were defined by electron-beam lithography (NanoBeam nB3) (Fig.1(b)). The molecular weight of the PMMA (950k) was chosen so that the required dose for development was lower than that of the NER. Then, hydrophilic SiO_2 insulator and Pt electrode layers were deposited by sputtering. Since the nano-valves will be switched by electrostatic fields from the Pt electrodes, the inner walls of the nano-valves must be insulated (Fig.1(c)). As shown in Fig.1(d), the top of the NER was exposed using chemical-mechanical polishing (CMP). The resist sacrificial layers were then removed (Fig.1(e)). Finally, we deposit Si_3N_4 as electrode top insulation layer. (see Fig.1(f)). The 20-nm thick nitride layer also has the effect of reducing the nano-valve diameter by 40 nm.

A cross section scanning electron micrograph (SEM) image of the on-chip fluidic channel is shown in Fig.2(a). A 1.5 μm wide and 800 nm high fluidic channel was formed on the SiO_2/Si substrate and the nano-valves were visible on the top channel surface. The SEM image of the 10 nm diameter nano-valve is shown in Fig.2(b). The switchable on-chip nano-valve arrays may be utilized in future integrated biochips for electrolyte sensing, drug-release and selective-permeable membrane constructions.

References

1. Bin Zhu, Jingjian Li, Qingwei Chen, Rui -Guo, et al., Phys. Chem. Chem. Phys, 12 (2010) 9989-9992.

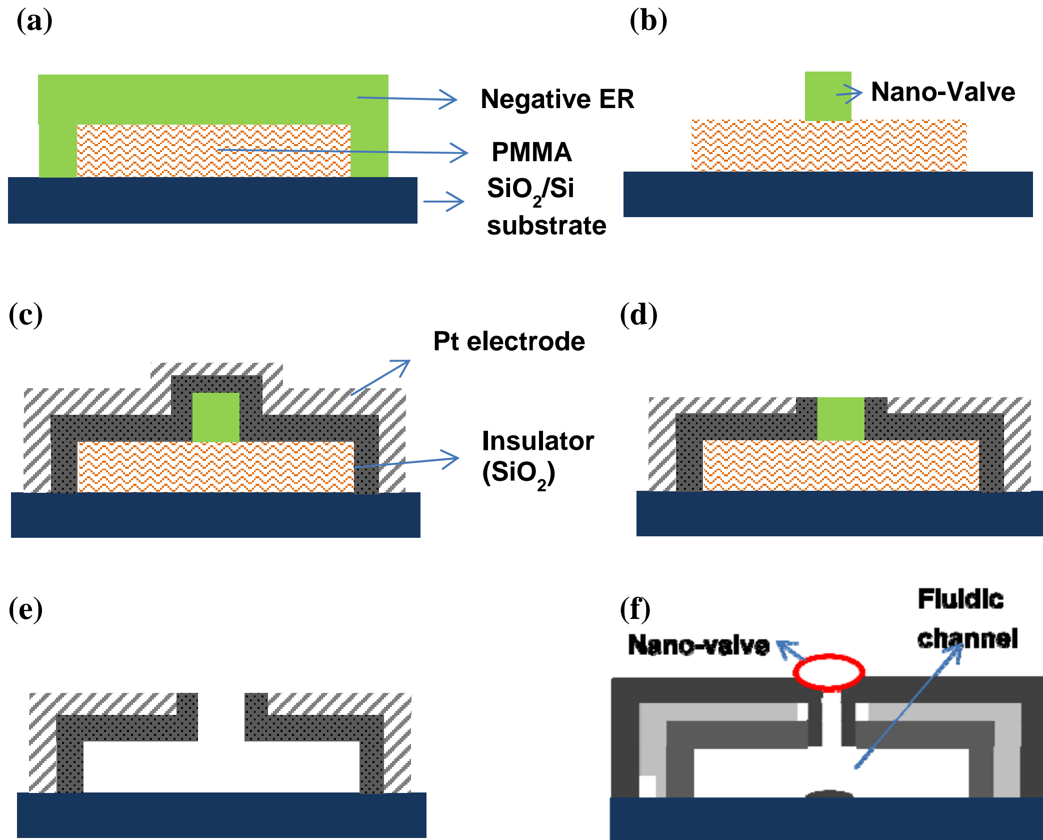

Fig.1. Schematic diagram of the self-aligned double layer resist processing technique. (a), (b) NER/PER double layer resist, (c) SiO_2/Pt layer sputter deposition (d) Nano-valve opening by CMP, (e) E-beam resist removal, and (f) Si_3N_4 top insulator deposition.

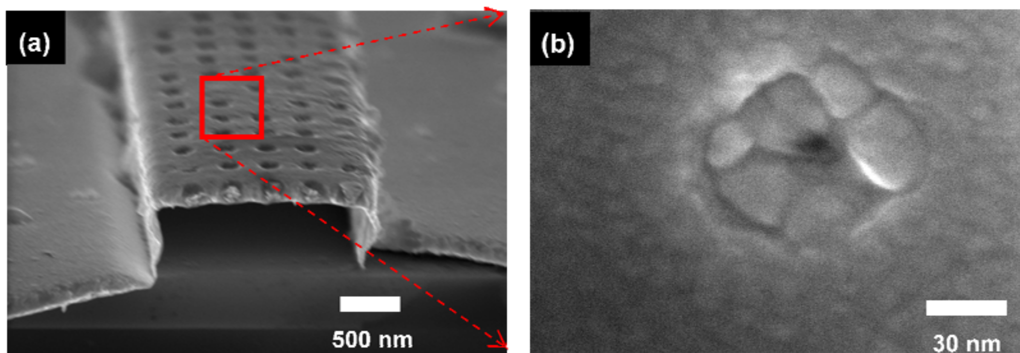

Figure 2. SEM image of the on-chip fluidic channel. (a) Cross-sectional view, (b) 10 nm diameter electrostatic nano-valve (top view).