Di-block Copolymer Guided Patterning of Graphene

Duyoung Choi[1], Cihan Kuru[1], Chulmin Choi[1], Kunbae Noh[2], and Sungho Jin[1]

[1]*Materials Science and Engineering, University of California, San Diego, La Jolla, CA 92093, USA*

[2]*Cheil Industries Uiwang R&D Center, Uiwang-si, Gyeonggi-do, Korea*

jin@ucsd.edu

Abstract

Graphene has significant potential for applications in electronics and various other related devices, but cannot be used for effective field-effect transistors operating at room temperature because it is a semimetal with a zero bandgap[1]. Processing graphene sheets into nanoribbons with several nanometer widths can open up a bandgap that is large enough for room-temperature transistor operation, but nanoribbon devices often have low driving currents or transconductances[2]. Moreover, practical devices and circuits would require the production of dense arrays of ordered nanoribbons, which remains a significant challenge. Here, we report the production of a new graphene nanostructure that can open up a bandgap in a large sheet of graphene to create a semiconducting thin film. The patterned graphene is prepared using block copolymer lithography and can have periodicities. Such nanostructuring process can effectively open up a conduction bandgap in a large piece of graphene. The block copolymer lithography fabrication of patterned graphene layer is an intrinsically scalable approach and can therefore enable a continuous semiconducting graphene thin film for fabrication of integrated devices/circuits with characteristics designed to meet specific circuit requirements[3].

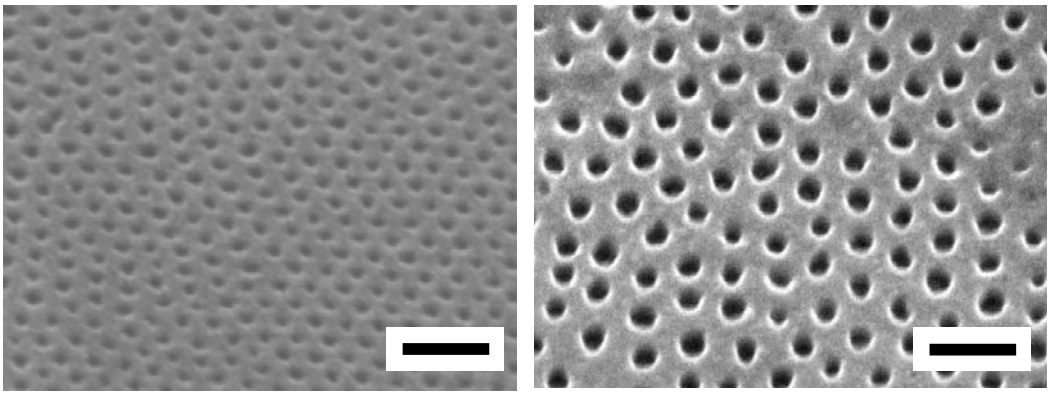
In this report, we demonstrate successful fabrications of ordered nanopore patterns directed on a graphene substrate by hexagonally patterned di-block copolymer layer placed on the SiO_2 film surface. A 20-nm thick silicon oxide (SiOx) film is first deposited onto graphene as the protecting layer and also as the grafting substrate for the subsequent block copolymer nanopatterning. The polystyrene-b-poly(4-vinylpyridine) (PS−P4VP) (P(S-b-S4VP)) block copolymer thin film with cylindrical domains normal to the surface is then fabricated and used as the etching template, and a reactive-ion etch (RIE) process is used to punch holes into the graphene layer. The availability of such patterned graphene will also provide an interesting system for fundamental investigation of transport behavior in the highly interconnected graphene network, and will enable exciting opportunities in sensitive biosensors and a new generation of spintronics devices. The nanopore formation process and the results of microstructural analysis will be described, and the scientific and technological implications will be discussed.

---

[1] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, Nature Nanotech. **3** 654 (2008).

[2] L. Y. Jiao, L. Zhang, X. R. Wang, G. Diankov, and H. J. Dai, Nature **458** 877 (2009).

[3] Y. W. Son, M. L. Cohen, and S. G. Louie, Nature **444** 347 (2006).



(a) (b)

Figure 1: SEM image of a nanopatterned graphene structure: (a) PS-b-P4VP block copolymer layer on SiO_2 thin film (before solvent annealing), (b) nanopatterned graphene surface. The pores have 15~30nm diameter and 20~30nm neck width after removing the top SiO_2 mesh mask. Scale bars, 100 nm.