Super selective silicon cryo-etching for nano-scale pattern transfer with block copolymer lithography

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One the biggest challenges to high resolution block copolymer (BCP) lithography is high fidelity plasma pattern transfer. High fidelity arises with high selectivity and thin passivation layers. We investigate the nanoscale application of cryogenic SF_6/O_2 silicon etching-- shown to deliver high selectivity with a thin passivation layer in micron scale features[1,2] as an option for BCP lithography pattern transfer, With a detailed study of the mechanisms controlling the process, we down to single digit nano (sub-10 nm) dimensions using block copolymer masks.

Previously we showed the process allowed high selectivity over a nanoimprint resist and ZEP-520 to achieve 10-20 nm features.[3,4] However, selectivity needed to be improved for better transfer fidelity or deeper etches at 20 nm and below. Here, we study in detail how to control the selectivity by understanding the etching mechanisms of both the mask and underlying silicon as a function of temperature, power, oxygen flow and feature size. For a given oxygen flow, highest selectivity and vertical profiles are achieved with lower temperature and a fine control of the bottom electrode power as demonstrated for 1.5 μm sized features (Figure 1). For small features, selectivity is reduced due to reactant transport reduction. Yet, with the appropriate low power recipe, we can increase selectivity for silicon with ZEP-520 from 7:1 to 10:1, a significant increase and a high selectivity for small features with thin masks. The process is then extended to pattern BCP created patterns into silicon. Fig. 2 shows 20 nm silicon holes etched and 20 nm fins both etched using a PS mask created by block copolymer lithography. In the former case, the BCP system is PS-PVP while in the latter, it is PS-PEO. Selectivity with the sub-16 nm mask was about 4:1. Profile and selectivity as a function of process condition and mask shape will be shown for 10 - 40 nm features. The process will be compared to HBr and SF_6/C_4F_8 etching of nanoscale features.

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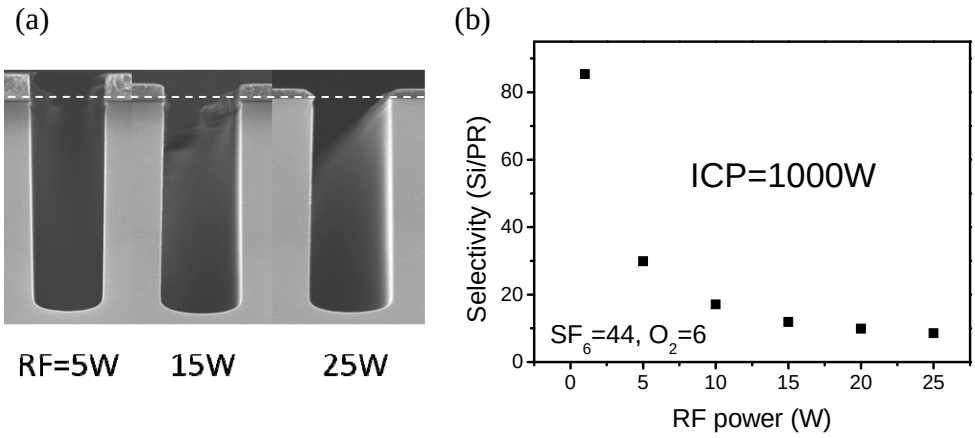

Figure 1. Lowering RF power in 1.5 μm features reduces the photoresist mask etching rate (notice mask height above black dotted line) and has little effect on Si etch rate, hence greatly increasing selectivity.

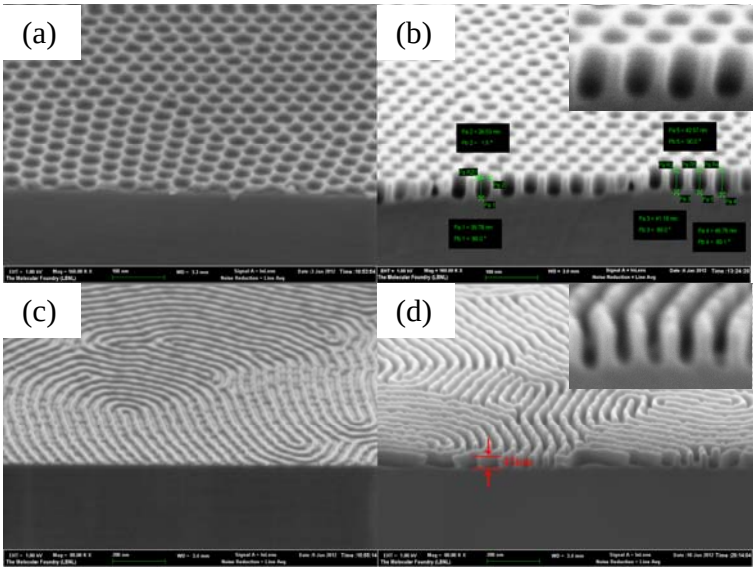

Figure 2. Pattern transfer into silicon with PS mask. PS mask formed from PS-PEO before etching (a) and after (b) to form 20 nm holes. PS mask formed from PS-PVP before etching (c) and after (d) to form 20 nm fins. Insets shows a closeup of the 20 nm etched features at the edge of the pattern.

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