# Employing Nano Imprint to Fabricate Space-Charge-Limited Transistors (SCLTs)

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Solution-processed organic transistors are promising for low-cost and large-area flexible electronics. We successfully demonstrated a vertical-channel solution-processed organic transistor, named as space-charge-limited transistor (SCLT), to have promising transistor characteristics [1]. An SCLT is similar to a vacuum tube triode whose structure is shown in Fig. 1(c). To have simultaneously a large current density and a good base control, the base metal should have high density openings with well-controlled diameter [2]. Previously the openings of the base metal fabricated by utilizing the self-organized polystyrene (PS) spheres as hard mask were easily accumulated to form large holes, causing enhanced leakage current and other issues such as uniformity and reproducibility.

To facilitate the real application of SCLT, a well-ordered nanometer pore structure is required, and we propose use both interference lithography and nanoimprint technology for patterning. Firstly, the stack layers of anti-reflection coating (ARC)/aluminum/polymer insulator (cross-linked poly(4-vinyl phenol), PVP) on an ITO glass substrate is prepared as shown in Fig. 1(a). Interference lithography is employed to generate a photo-resist hole array pattern on a Si substrate [3], which is further transferred to PDMS. The nanostructure on PDMS mold is gas-pressure imprinted onto the ARC film. Fig. 2(a) shows the obtained hole array etching mask with good uniformity over a large area. The nano-pore structure is then transferred to aluminum metal, as shown in Fig. 2(b) by a simple wet etching process. After $O_2$ plasma treatment, the vertically-oriented PVP cylindrical nano-pores are formed as shown in Fig. 2(c). Subsequent depositions of poly(3-hexylthiophene) (P3HT) as the active material and $MoO_3$ / Al to complete the SCLT are carried out.

The output characteristics ($J_C$-$V_{CE}$ curves) and the transfer characteristics ($J_C$-$V_{BE}$ curves) of the fabricated imprint SCLT are shown in Fig. 3(a) and (b),

respectively. We obtain an on current as 0.35 mA/cm$^2$ and an on/off current ratio around 3000 at $V_{CE}$ as 1.8 V. Compared to our previously published device performance, the performance is not the best, however, better than our first reported SCLT [4]. In summary, the first successful use of interference lithography and nano-imprint technology to fabricate SCLT is demonstrated. Further process optimization is being carried out to improve performance.


[1] Y-C Chao, *et. al.*, Organic Electronics, vol. 12, Issue 1, pp. 78-82, 2011.

[2] Y-C Chao, *et. al.*, Appl. Phys. Lett., 98,203303, 2011.

[3] Y-P Chen, *et. al.*, J. Vac. Sci. Technol. B, 27(6), pp. 2951-2957, 2009.

[4] Y-C Chao, *et. al.*, Appl. Phys. Lett. , 88, 223510, 2006.


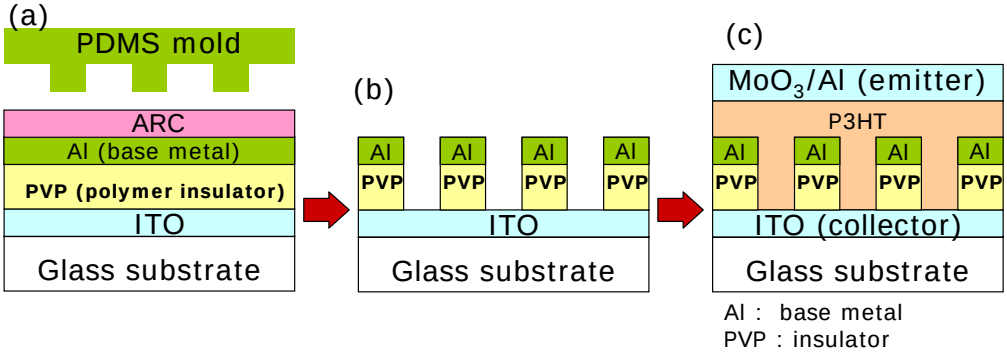


Fig. 1 Schematic diagram showing the fabrication of SCLTs: (a) key step of utilizing nanoimprint, (b) after etching, (c) final devices.

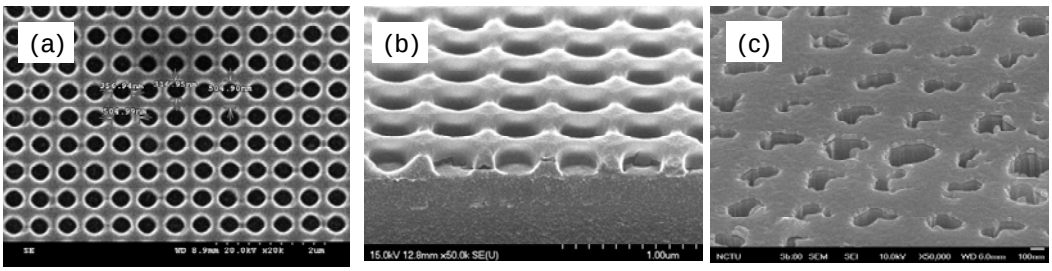


Fig. 2 SEM images of (a) hole array etching mask, (b) Al nano-pore structure after wet etching, (c) vertically-oriented PVP cylindrical nano-pores.

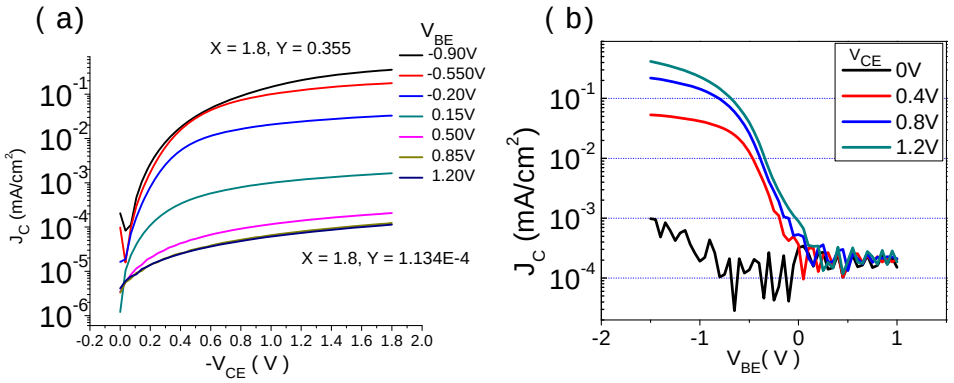


Fig. 3 Performance of imprinted SCLT: curves of (a) $J_C$-$V_{CE}$, and (b) $J_C$-$V_{BE}$.