

Nanolithography and pattern transfer of dense sub-10 nm lines

A. S. Jugessur, M. Yagnyukova and J. S. Aitchison

Emerging Communications Technology Institute, Faculty of Applied Science and Engineering, University of Toronto, Ontario, Canada M5S3G4

The patterning and transfer of ultra-small features in the nanometer regime on a wide variety of substrate materials have become an important area of research in recent years [1]. The main driver of this field has been the microelectronics industry where the transistors keep diminishing in size as predicted by Moore's law [2]. This trend has also benefited other scientific and technological areas involving the fabrication of nanodevices for a wide range of applications in sectors such as bio-medical, environment, energy, communications [3] and sensing [4]. As a result, the process development of sub-10 nm patterning and transfer of features have become very critical to ensure the realization of nanoscale devices.

In this report, electron beam lithography process development of sub-10 nm lines on 25 nm thick Hydrogen Silsesquioxane (HSQ) resist is investigated using a Vistec EBPG5000plus system at 100 kV. The exposed patterns are developed in CD26 using hot development technique at 50 ° C and ultrasonic agitation. Lift-off processes are developed and optimized to transfer the patterns on silicon substrate. The influence of several process parameters such as development temperature, exposure current, exposure dose, pattern density and pitch on the linewidth is investigated. Dense periodic lines of 4 nm wide with 25 nm pitch and 10 μm long, covering an exposed area of 100 x 100 μm have been achieved using a set of optimized process conditions. Figure 1(a) and (b) shows the 4 nm lines exposed using electron beam lithography (beam current: 50 pA, dose: 22,000 $\mu\text{C}/\text{cm}^2$) at 100 kV and lift-off result on a silicon substrate respectively.

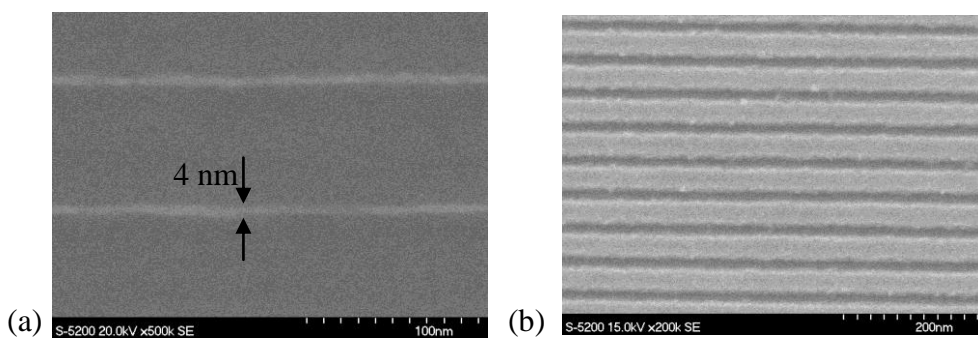


Figure 1: (a) 4 nm lines exposed on HSQ using electron beam lithography, (b) lift-off of sub-10 nm lines on silicon substrate

- [1] Grigorescut A. E., van der Krogt M.C., Hagen and Kruit P., *Microelectron. Eng.*, 84, p. 822–824 2007
- [2] Seisyan R. P., *Nanolithography in Microelectronics: A Review, Technical Physics*, 56, No. 8, p. 1061-1073 2011
- [3] Jugessur A. S., Dou J., Aitchison J. S., *Journ. of Vacuum Sci. and Tech.* B28, 6, C608-C6010 2010
- [4] Jugessur A. S., Dou, J., Aitchison J. S., De La Rue R. M and Gnan M., *Microelectron. Eng.*, 86, 1488-1490 2009