Proof of 50keV Electron Multi-Beam Writing at 0.1nm Address Grid

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Printing results [1] of a proof-of-concept 50keV electron multi-beam mask exposure tool (eMET POC) as achieved on 150mm Si monitor wafers and 6" mask blanks are presented. The realized system (Fig. 1) with a 200x reduction column provides 256k (k=1024) programmable beams of 20nm beam size. 24nm HP resolution is demonstrated (Fig. 2a), any angle lines (Fig. 2b), as well as complex OPC (Fig. 2c) and ILT patterns (Fig. 2d). As part of eMET POC acceptance tests, 50nm lines were printed with periodicities altered from 100.0nm in steps of 0.1nm to 109.9nm. Figure 3a shows, as an example, 50nm lines exposed with 101.3nm pitch and with 109.8nm pitch. CD-SEM measurements show pitch deviations as low as 0.23nm 3sigma (Fig. 3b) and 50nm CD deviations of 1.6nm 3sigma (including measurement errors). These results demonstrate 50keV electron multi-beam writing at 0.1nm address grid.

[1] Elmar Platzgummer, Christof Klein, and Hans Loeschner, "Printing results of proof-of-concept 50keV electron multi-beam mask exposure tool (eMET POC)", Proc SPIE **8522**, 8522-52 (2012).
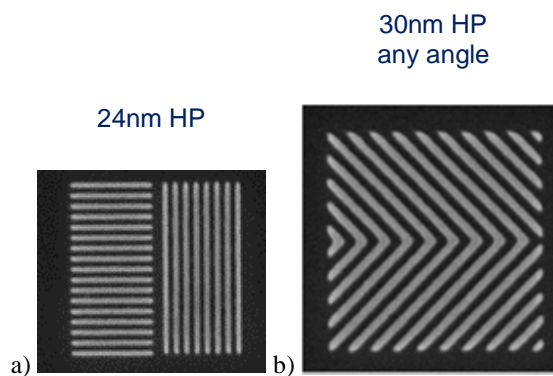
Figure 1: eMET POC

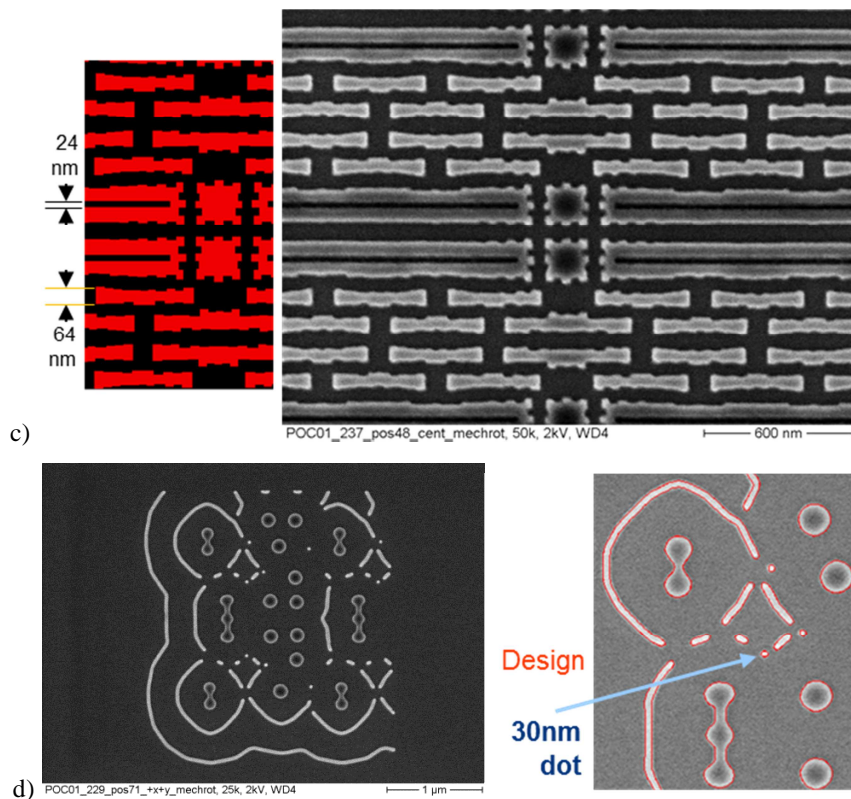

Figure 2: (see following page)

Figure 2: eMET POC printing results in 50nm HSQ negative resist, (a) 20nm HP lines in X and Y, b) any angle 30nm HP lines, (c) aggressive OPC pattern with 24nm smallest space, (d) ILT pattern with 30nm dot smallest feature.
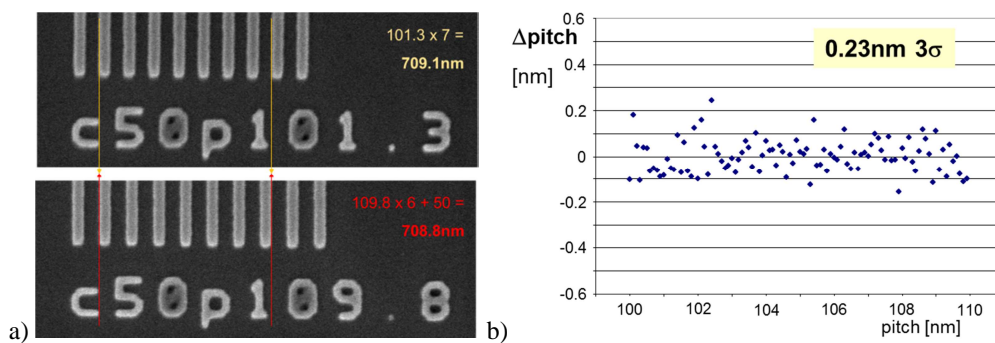

Figure 3: a) 50nm lines exposed in 50nm HSQ negative resist with 101.3nm pitch (above) and 109.8nm pitch (below). The signature below the 50nm line pattern, with "c50" for 50nm CD and "p10x.y" for pitch in nm, was written with 30nm line width and dot size, using programmable beams of 20nm beam size; b) Difference between measured pitch and design pitch vs. design pitch for pitch values between 100.0nm and 109.9nm in 0.1nm steps.