## NGL for NGL

## Next Generation Lithography for Next Generation Logic

## Yan Borodovsky

Portland Technology Development, Technology& Manufacturing Group, Intel Corp., Hillsboro, USA

## Abstract

Optical lithography provided patterning capabilities with unparalleled data transfer rates at defect densities approaching zero in high volume manufacturing, making semiconductor products ever more powerful, ubiquitous and affordable to everyone. The latest 22nm generation products manufactured by Intel using Optical Lithography count billions of Tri-gate transistors that have better performance and cost per transistor than any previous Intel Technology generations. With use of Pitch Division, Optical Lithography will be extended beyond he 22nm node, yet at some point Complementary Lithography which combines the best of what Optical Lithography and what is commonly referred to as NGL (Next Generation Lithography) will have to offer might become a more powerful manufacturing technique than Optical Lithography alone.

EUVL, EBDW and DSA are all under consideration to complement optical lithography. While their respective maturity differs significantly—with EUVL being the most mature—their rate of development as of late varies considerably. DSA is making fast inroads in the Lab-to-Fab transition, and massively parallel E-Beam tools ready to ship industrial prototypes with hundreds of thousands of beams writing in parallel.

Defectivity and required corresponding wafer metrology, sampling and disposition methodology needed for introduction of DSA and EBDW in HVM is yet to be developed. Absence of defect free mask that is protected from spurious contamination events by pellicle will require significantly different approach to wafer defectivity characterization than methodology and tools currently in use. EUVL on another hand might be able to offer defect free masks at the time of its HVM insertion. There are also significant efforts on the way to develop pellicle for EUVL mask but its availability for the time of EUVL HVM insertion is still an open question.

Logic chips are intolerant of even the smallest defects, and methodology challenges that address defectivity issues for maskless or pellicleless manufacturing are yet to be considered, understood and resolved. This presentation will focus on defectivity concerns specific to the above-stated NGLs, and possible means to address those concerns in a Logic product manufacturing environment.