Process Monitoring of an Electron Beam Lithography Process for Silicon Photonics in a University Facility

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Electron beam lithography is used to fabricate silicon photonics for diverse applications including nano-optomechanics, biosensing, nonlinear optics, and integrated photonics[1]. Ensuring process consistency over time is challenging, as few university fabrication facilities can afford specialized metrology such as CDSEM or overlay metrology tools utilized in commercial fabrication. To fill this void, we have developed simple process monitoring using ordinary optical and scanning electron microscopes, with custom image-processing and measurement software. It was previously shown that using the highly accurate writing pitch of e-beam lithography coupled with relatively simple image processing and calculation software, nanometer-scale accuracy is easily achievable from ordinary SEM images.[2] Keys to consistent, accurate measurements are: use of the inherent accuracy of localized pattern scaling in the e-beam writing process from calibration with the e-beam writing tool's stage laser interferometer, and if possible, use of symmetry in test structures to simplify edge position determination.

One process characteristic we monitor is layer-to-layer overlay, using a pattern of symmetric interdigitated lines on alternate layers. A key feature is that shapes are spaced a known distance apart on the same layer; these are used for scaling calibration of each image (Figure 1). Measurements are faster and more accurate than optical verniers and occupy less wafer surface area than grating structures. We verified the accuracy of this method by using single-layer calibration patterns with intentional feature offsets (Figure 2). Measurement of CD is more challenging for several reasons: it is not possible to avoid imaging and edge-finding threshold effects on the measurement, simple analytic SEMs generally have poor scaling calibration, and after etching our SOI wafers have large areas of exposed insulating surface which charges during SEM imaging. We reduce these effects by measuring a series of small gratings designed at a fixed pitch and varying duty cycle. Again the grating pitch is used to calibrate the scaling of each image.

We present design considerations, imaging and analysis options, measurement results from calibration structures, limitations, and process monitoring data from fabrication of silicon photonics chips. These metrology capabilities have allowed us to fabricate silicon photonics devices consistently over many months (Figure 3). While not a substitute for general-purpose metrology tools, we show that for this application, even simple tools and image analysis software can be useful in providing valuable process monitoring data.

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[1] R.J. Bojko, et. al. J. Vac. Sci. Technol. B **29**, 06F309 (2011)
[2] M. Rooks, Analysis of electron-beam deflection noise with open-source software. EIPBN 2010.

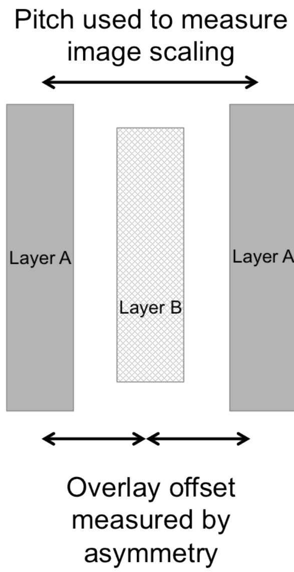

Figure 1. Structure used to measure layer-to-layer overlay

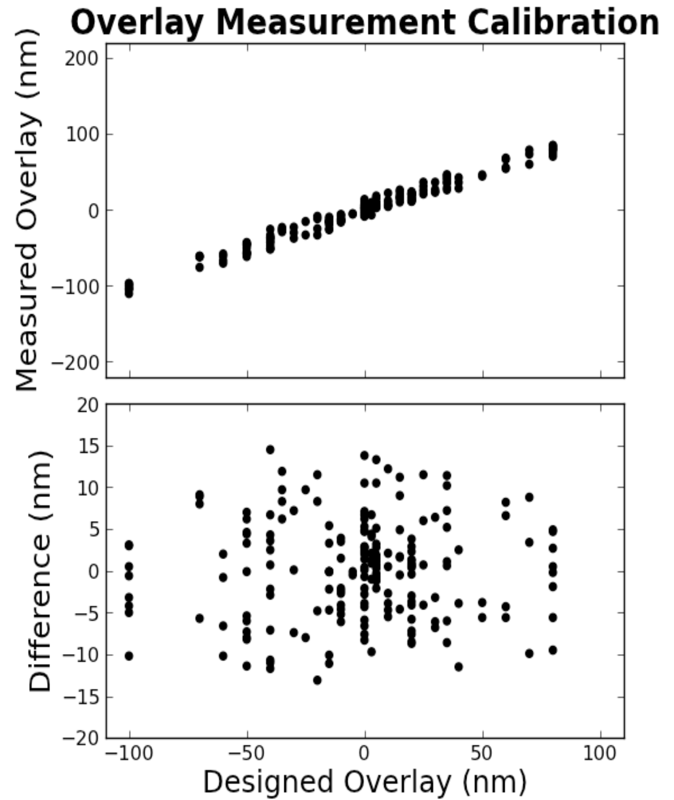

Figure 2. Calibration of Overlay Measurement

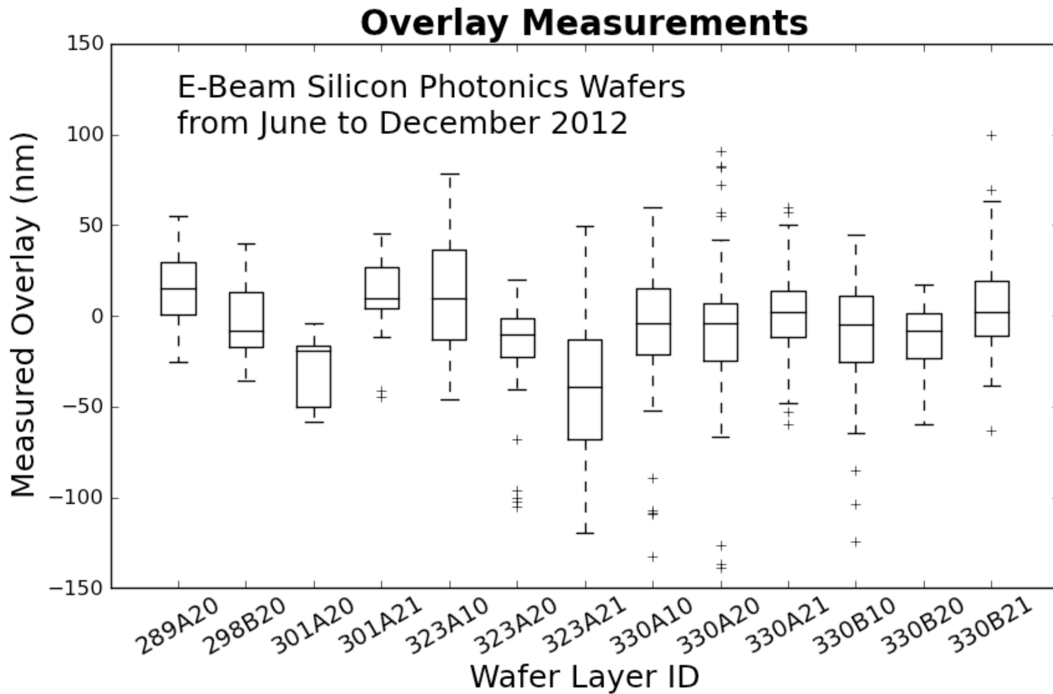

Figure 3. Overlay measurements for e-beam written silicon photonics wafers.