Contamination Mitigation from Salty HSQ Development for Nanoscale CMOS Device Patterning

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Continued CMOS scaling has sparked an interest in fabricating Si-based devices with features in the sub-30 nm pitch regime. This resolution is not easily obtained even with electron beam lithography (EBL) due to resist limitations. Hydrogen silsesquioxane (HSQ) developed with an aqueous solution of NaCl and NaOH (a.k.a. salty develop) has demonstrated high spatial resolution[2], achieving clean 15nm half pitch features (Fig. 1). Contamination concerns, however, have prevented the application of salty develop to Si CMOS device integration in laboratories with rigorous contamination controls. In this paper we detail the results of a study aimed at reducing the residual contamination of salty developer to a level suitable for continued processing in a CMOS device research line.

Use of any sodium (Na) containing material is a cause for concern in CMOS processing environments. If left untreated, a salty developed Si wafer shows a high concentration of Na, as measured by total reflection x-ray fluorescence (TXRF, Fig. 2). We found that a rigorous deionized water rinsing protocol immediately after salty development can reduce the Na level below the TXRF detection limit. It is widely known that TXRF has poor sensitivity to Na. The fact that we were able to detect Na on wafers that did not receive the rinsing protocol is evidence that the residual Na level was significant. To detect small amounts of Na^+, we measured contamination from displacement currents observed across the dielectric of a capacitor (Fig. 3). Due to the ubiquitous presence of Na in the environment, a sensitive measurement could detect Na on control wafers. As a result, we compared 3 different capacitors consisting of (a) a thermal oxide that has been exposed to salty developer and water cleaned, (b) an identically processed wafer that used TMAH developer in place of salty developer, (c) a reference wafer. The capacitance data from the 3 wafers is shown in Fig. 3 and analyzed in Table 1. The Na^+ in the SiO_2 is essentially the same on all 3 wafers and within the limits established for processing in our CMOS line. This leads us to conclude that the Na^+ uptake from salty developer after water cleans is no more than from other process steps and within the noise of this capacitive measurement.

Salty developer is currently not commercially available, requiring users of this process to mix the developer from standard chemicals. We discovered trace amounts of some metals, particularly iron (Fe) and nickel (Ni), on our wafers after salty development. These heavier elements were readily detected by TXRF and measured concentrations slightly above the limits for our lab (Fig. 2). We attempted several wet metal cleans post develop; none of them resulted in reliable reduction of the contamination. Instead, we reduced the contamination by choosing high purity, low metal content chemicals for the developer solution. While traces of Fe and Ni could still be measured, their concentration was reduced by an order of magnitude and consistently measured well below our requirements.

Following these protocols we were able to fabricate CMOS capacitors with high resolution features. Structural and electrical data from these devices will also be discussed as further examples that the post develop contamination has been reduced to acceptable levels.

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[2] J. K. W. Yang and K. K. Berggren, J. Vac. Sci. Technol. B 25 (6), 2025-2028 (2007).

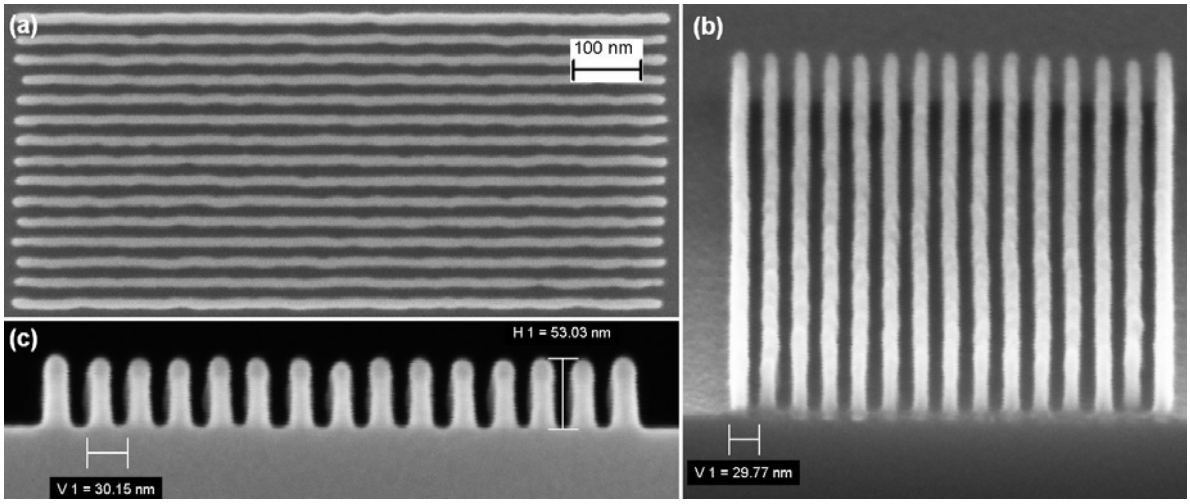

Figure 1: Salty developed line/space pattern written by EBL in HSQ at15nm half pitch after pattern transfer RIE into bulk Si. Images taken at different magnifications. (a) Top-down SEM image. (b) Tilted cross-section SEM image. (c) Cross section SEM image. Etched lines show approximately 50nm height.

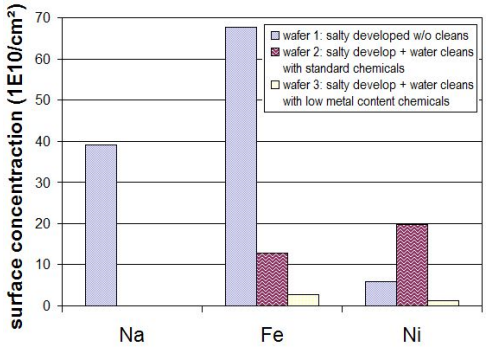

Figure 2: TXRF data of sodium (Na), iron (Fe), and nickel (Ni) from 3 salty developed wafers. Without cleans after salty development, a sizable Na concentration is measured (wafer 1). The Na peak in TXRF vanishes upon rigorous water cleans (wafers 2, 3). If salty developer is made from standard grade chemicals, we also find Fe and Ni in TXRF (wafers 1, 2; whose developers were made from different chemical vendor sources). This contamination is minimized by making the salty developer from high purity, low metal content chemicals (wafer 3).

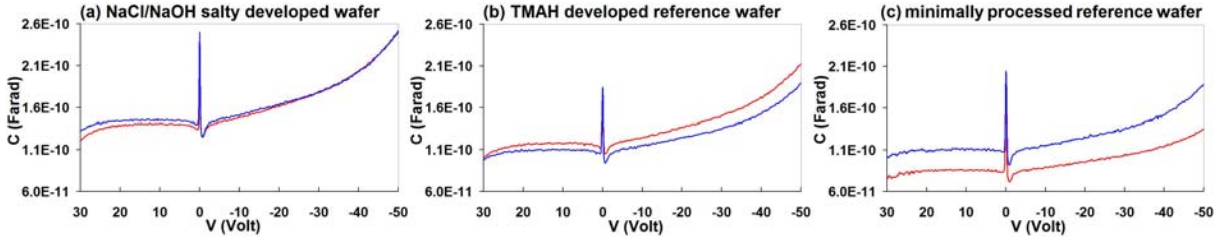

Figure 3: Capacitance vs. bias voltage for 3 different wafers with 100nm thermal silicon oxide. Each plot shows 2 traces, which are taken from different aluminum (Al) metal contacts on the same wafer. (a) salty developed wafer, with developer mixed from low metal content chemicals, (b) TMAH developed reference wafer: uses standard TMAH developer in place of salty developer, and (c) minimally processed reference wafer. The peak near 0V is associated with Na^+ ions in the dielectric.

wafer	data trace	mobile ion concentration
salty developed	1: red	4.38E+10 / cm²
	2: blue	8.10E+10 / cm²
TMAH developed	1: red	5.43E+10 / cm²
	2: blue	6.48E+10 / cm²
reference	1: red	8.87E+10 / cm²
	2: blue	8.11E+10 / cm²

Table 1: Na^+ ion concentration for the 6 data traces in Fig. 3. No significant difference in the Na^+ ion concentration between the salty developed and the reference wafers. The mobile ion concentration is extracted by integrating the area under the capacitance peak near 0V bias less the background capacitance and subsequently normalizing this charge by the size of the metal contact $A_{contact}$ and the proton charge e.

$$\text{mobile ion concentration} = \frac{Q_{mobile}}{eA_{contact}} = \frac{1}{eA_{contact}} \int_{peak} (C - C_{backgnd})\, dV$$