MEMRISTIVE NANODEVICES: MECHANISMS, PROMISES AND CHALLENGES

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The desire to continually improve computing systems drives both the relentless scaling of existing silicon integrated circuit technology and the search for new technologies. To be relevant, new devices must be both nanoscale and extremely capable. Memristive nanodevices (RRAM) appear to fulfill these requirements. These devices are electrical resistance switches that can retain a state of internal resistance based on the history of applied voltage and current. Memristive devices can store and process information, and offer several key performance characteristics that exceed conventional integrated circuit technology [1]. An important class of these devices are two-terminal resistance switches based on ionic motion, which are built from a simple conductor/insulator/conductor thin-film stack. I will first describe the switching mechanisms [2, 3] of metal-oxide switches and a related family of nanodevices [4], along with their potential applications [5, 6]. Then the promises and challenges [1, 7] with respect to using these devices will be discussed together with some possible solutions [8-11]. Among different switching materials, TaO_x has stood out as one of the leading electrical switching materials, with record-high endurance (10^{12}) and switching speed (0.1 ns) [3]. The origin of the high endurance of TaO_x switches and the material selection criteria for high performance switches [9] will be discussed. The switching mechanism of TaO_x devices will be examined by locating and anatomizing the nanoscale conduction channel buried inside the device, as shown in Figure 1 [3]. Despite the encouraging electrical performance demonstrated in TaO_x based memristive switches, they display a linear current-voltage relation in the low resistance state (Figure 2c), which limits their applications in large passive crossbar arrays without select devices. Engineering high nonlinearity into the current - voltage relation of TaO_x nanodevices by using an oxide heterostructure will be demonstrated, as shown in Figure 2d [10].

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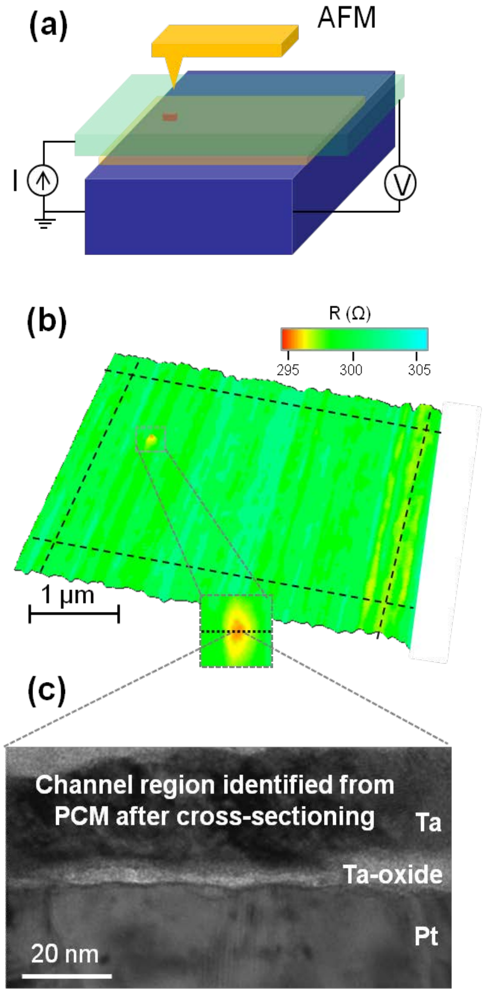

Figure 1: Identification and visualization of the conduction channel. (a) Schematic illustration of Pressure-Modulated Conductance Microscopy (PMCM), for which a non-conducting AFM tip applied pressure to the top electrode while the resistance of the device was monitored, yielding a resistance map as a function of tip position. (b) The resistance map of a TaO_x based memristor, where the red dot (resistance decrease), highlighted by the dashed square in the magnified inset, corresponds to the conduction channel. The color scale represents the measured resistance values. The conduction channel was cross-sectioned by FIB across the center (indicated by the black dashed line in the inset). (c) TEM image of the conduction channel region identified from PMCM.

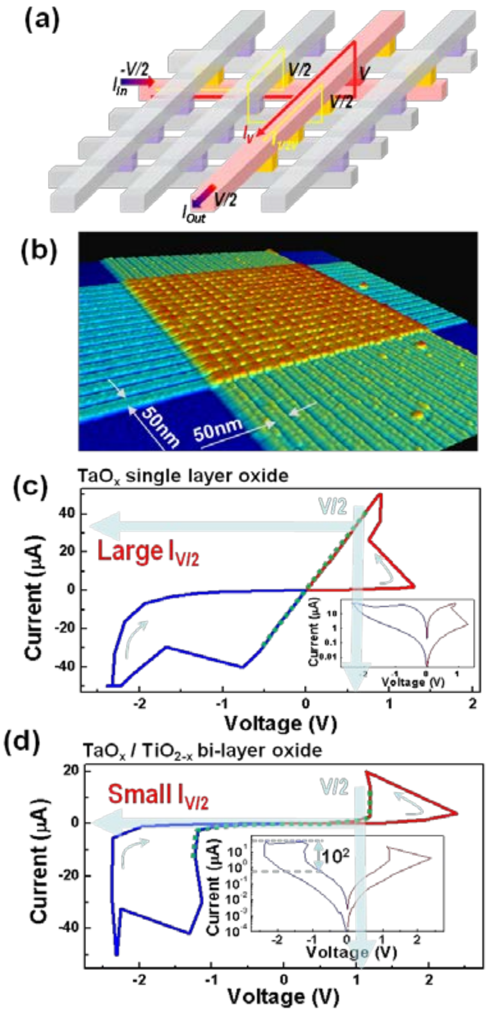

Figure 2: crossbar array and current voltage loops of nanodevices. (a) schematic illustration showing the sneak path current through the half-selected memristors (b) atomic force microscopy image of a crossbar array with 50 nm half-pitch fabricated by nanoimprint lithography. (c) switching loop from a Pt / TaO_x / Ta 50 nm × 50 nm crosspoint device, showing linear *IV* curve in the ON state. (d) switching loop from a Pt / TaO_x / TiO_{2-x} / Pt 50 nm × 50 nm crosspoint device, showing nonlinear *IV* curve in the ON state.