Integration of Planar Memristors with CMOS for Hybrid Circuits

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With silicon based technologies approaches the scaling limit, CMOS/nanodevice hybrid systems offer another opportunity to go beyond the Moore's Law. Emerging nanoelectronic devices such as resistive switches (also known as memristors or memristive devices) have been integrated with CMOS circuits for FPGA-like reconfigurable circuits [1] and neuromorphic network. [2] However, from a device perspective, the performance of hybrid circuits can be greatly improved by adopting better devices and integration technologies. Here we demonstrated a memristor/CMOS hybrid circuit with planar devices [3] whose bottom electrodes were embedded into the CMOS substrates. The new device geometry has led to much lower voltage switching behavior.

Fig. 1 shows the integration process. Planar memristor crossbar arrays were fabricated using nanoimprint lithography on top of a foundry made CMOS substrate. The electrical connection was made between tungsten vias in CMOS and contact pad in crossbar arrays. Due to dishing effect in chemical mechanical polish (CMP), the top surface of the vias was 75 nm below that of the CMOS substrate. By carefully designing the process parameters, we were able to achieve patterning over this non-flat surface and also embedded a thick (77 nm) bottom electrode into the TEOS layer.

Fig. 2 shows optical and SEM images of the fabricated planar crossbar memristor arrays on top of the CMOS substrate. Fig. 2a shows a complete planar memristor routing network for one die, with bottom (darker) and top (brighter) electrodes wired up to the CMOS circuit beneath. Fig. 2b shows a 2 by 3 planar memristor array of 100×100 nm^2 devices with 77 nm thick bottom electrodes embedded in the TEOS layer.

For comparison, we also fabricated non-planar 'ribbed' devices (Fig. 3). The difference in the top electrode topography changed the electric field distribution hence affect the device performance. In addition to the proved longer endurance [3], a planar device required much lower forming and programing voltages than a "ribbed" device (Fig. 4). This reduced programing voltage was attributed to the thicker electrodes hence smaller series resistance from the metal nanowires. Furthermore, the uniformity of the forming and programing voltage of the planar devices were found to be significantly higher than the "ribbed" devices. For example the variation of the programming voltage for a planar device with 14 nm thick bottom electrode was within 15% while that for a ribbed device of the same geometry was 38% (Fig. 4d). Using a thicker bottom electrode further enhanced the device uniformity. Finally, we addressed those memristors integrated in the hybrid circuits through I/O paths at the edge of a die. The forming and programing voltages remained at the same level even went through the long nanoscale routing wires. The low voltage and uniform switching behavior of planar devices reached CMOS compatibility for hybrid circuits.

[1] Xia, Q.; Robinett, W.; Yang, J. J. *et al. Nano Letters* 9, 3640-3645 (2009)
[2] Jo, S. H.; Chang, T.; Ebong, I *et al. Nano Letters* 10, 1297-1301 (2010)
[2] Xia, Q.; Pickett, M. D.; Yang, J. J. *et al. Nanotechnology* 22, 254026 (2011)

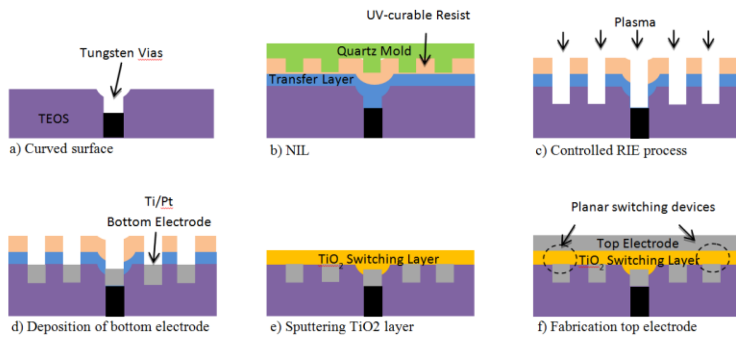

Figure 1. Schematic of the integration process.

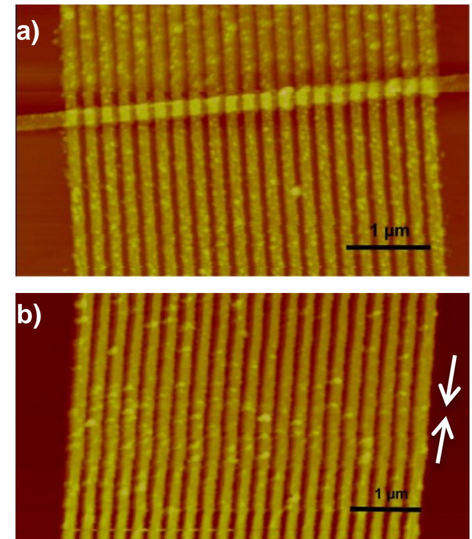

Figure 3. AFM images: (a) "Ribbed" Memristor device with 14 nm thick electrode. (b) Planar Memristor device with 77 nm thick electrode, the bottom electrode is barely visible in between the arrows.

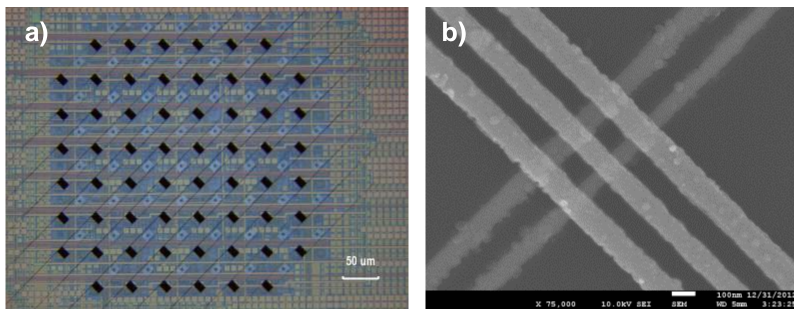

Figure 2. (a) Optical image of resistive switching array fabricated on top of the CMOS substrate (b) SEM image of planar crossbar memristors with a $100 \times 100\ nm^2$ junction area.

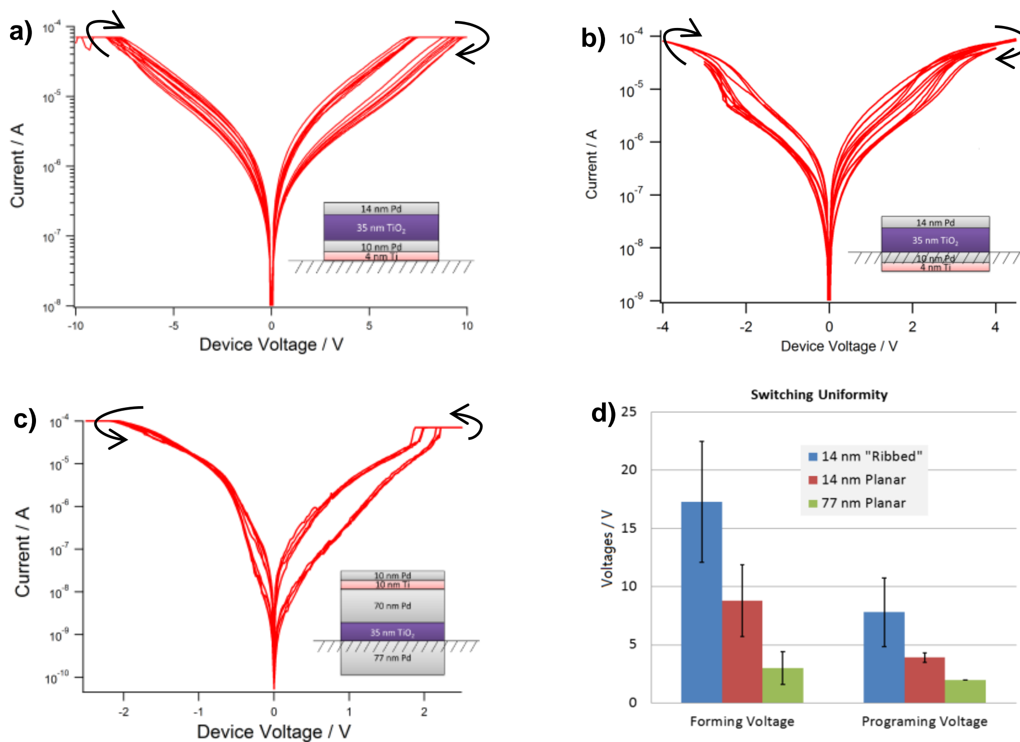

Figure 4. Comparison of switching behavior of non-planar device and planar device. (a) "Ribbed" device (14 nm thick electrode, forming voltage: -28V) (b) Planar device (14 nm thick electrode, forming voltage: -7V). (c) Planar Device (77 nm thick electrode, forming voltage: 3V).The planar geometry yields much lower forming and programing voltages. (d) Comparison of forming and switching voltages of different device geometry.