Fabrication of 18 nm split-gate charge trap memories by hybrid lithography (e-beam/DUV)

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Split-gate charge trap memory architectures (Fig. 1) are investigated to develop low-power and low-cost embedded memories due to their unique property of combining the nanocristal storage layer and split-gate configuration advantages [1,2]. Indeed, the use of nanocristal storage layer limits the impact of stress-induced leakage current (SILC) on data retention [3] and allows memory downscaling. Moreover, the use of a split-gate design enables to meet low-power, high-speed and reliability requirements [4].

In this study, we demonstrate the possibility to achieve sub-32 nm split-gate memories on 8-inch wafers with a good reliability. For this purpose, a double hybrid lithography (e-beam/DUV) patterning process have been developed in order to define the two gate levels, using a negative chemically amplified resist [5--8]. E-beam exposures were carried out on a Leica VB6UHR 100KV from Vistec, optical lithography on a KrF ASML stepper (248 nm). The initial gate resist dimensions were between 40 and 350 nm. The main difficulty was to perform a patterning strategy enabling to control the alignment between the memory gate (MG) and the select gate (SG), see Figure 1, because this overlap determines the memory gate length (L_{MG}).

In the end, we have demonstrated that it could be possible to fabricate sub-32 nm split-gate charge trap memories (Fig. 2) with silicon nanocrystal (Si-nc), silicon nitride (Si3N4) and Si-nc/SiN charge trapping layers. At present our current best result (L_{MG}) is close to 18 nm (Fig. 2), which is a state-of-the-art result for embedded memories. Moreover, these memories exhibit good electrical properties.

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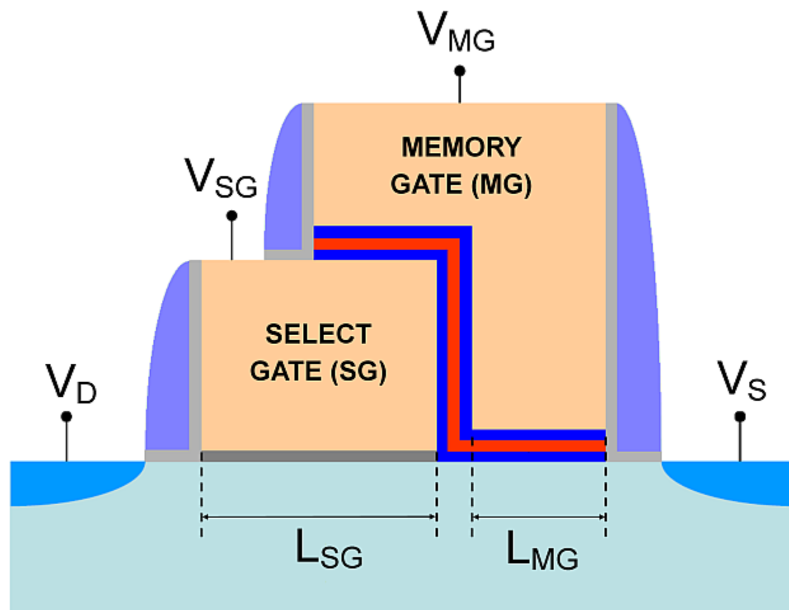

Figure 1: Schematic of a split-gate charge trap memory

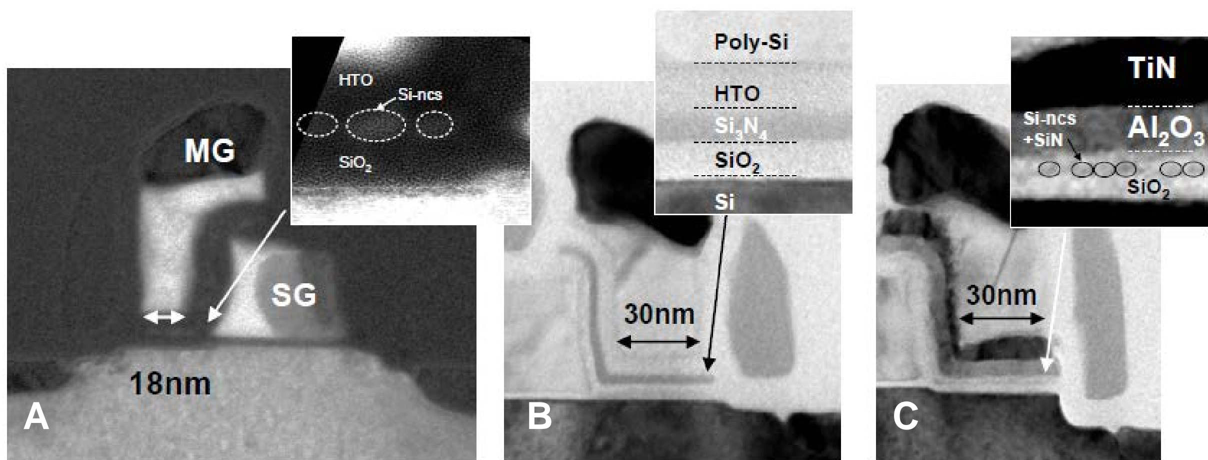

Figure 2: TEM cross sectional images of split-gate charge trap memories with different memory gate stacks; (A) Si-nc, (B) Si3N4 (C) Si-nc/SiN charge trapping layers.