

MAPPER progress towards a High Volume Manufacturing EBDW system

G. de Boer^a, M.P. Dansberg^a, R. Jager^a, P.Kruit^b, J.J.M. Peijster^a, E. Slot^a,
S.W.H.K. Steenbrink^a and M.J. Wieland^a

^a MAPPER Lithography B.V., Computerlaan 15, 2628 XK Delft, The Netherlands

^a Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands

E-mail: p.kruit@tudelft.nl or marco.wieland@mappperlithography.com

MAPPER Lithography is developing a maskless lithography technology based on massively-parallel electron-beam writing with high speed optical data transport for switching the electron beams. In this way optical columns can be made with a throughput of 10 wafers per hour. By clustering several of these systems together, high throughputs can be realized in a small footprint. This enables a cost-competitive solution for either direct patterning or for complementary patterning approach [1, 2]. For a 10 wph throughput per unit, MAPPER will use 13,260 parallel electron beams, delivering 170 μ A to the wafer. To realize this large current at the wafer without blurring by Coulomb interactions MAPPER uses its patterned beam approach where each beam consists of 49 subbeams, see figure 1 [3].

The individual subbeams are switched on and off by the blanker. Subbeams that need to be switched off are deflected, and do not pass an aperture downstream. The blanker consists of 5 chips, one for each beam area, see figure 2. Each chip has a size of 6mm x 33mm, and contains the circuitry to receive the data for 2652 beams, each consisting of 49 subbeams. The data rate per beam is 3.5 Gbs. This data is transported to the chip through optical fibers, and photodiodes that are mounted onto the chip. The blanker chip is fabricated in 65nm TSMC CMOS. After fabrication by TSMC, MAPPER etches the 2652x49 through wafer holes. For the 1 wph tool we will only integrate one of these chips and use the central beams.

The data coming from memory is real-time corrected for beam to beam position errors and overlay related distortions. For the 10 wph tool this requires the resampling of 8 Tbyte in 4 seconds. In our design this is done with 1560 FPGA's. The data system for the 1 wph tool has been built and tested.

MAPPER is currently building up several tools of what we call the MATRIX platform.

In the mean time process development is done in an industry consortium led by with LETI in Grenoble, where one of the Asterix tools has been in operation for several years [4]. Results such as depicted in figure 3 are a result of this effort.

[1] E. Slot et al., Proc. of SPIE, Vol. 6921, 69211P, (2008)

[2] M.J. Wieland et al., Proc. of SPIE, Vol. 7271, 72710O1, (2009)

[3] M.J. Wieland et al., Proc. of SPIE, Vol. 7637, 76371Z (2010)

[4] L. Pain et al., Proc. of SPIE, Vol 7970, 79700Y (2011)

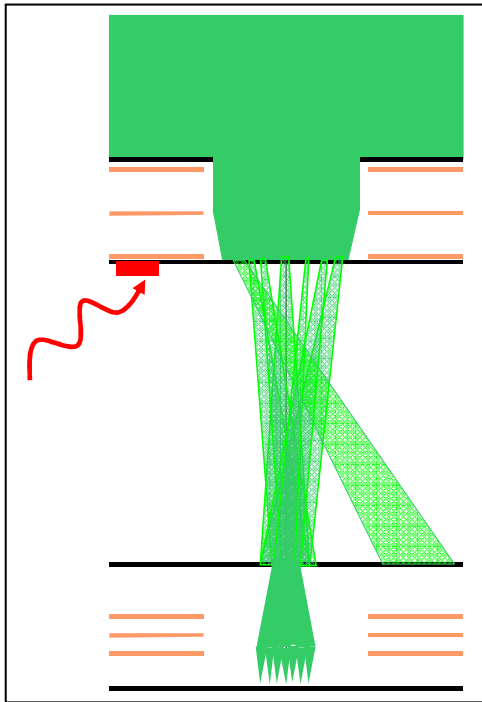


Figure 1. Schematic overview of the electron optical system for one of the 13,260 beams.

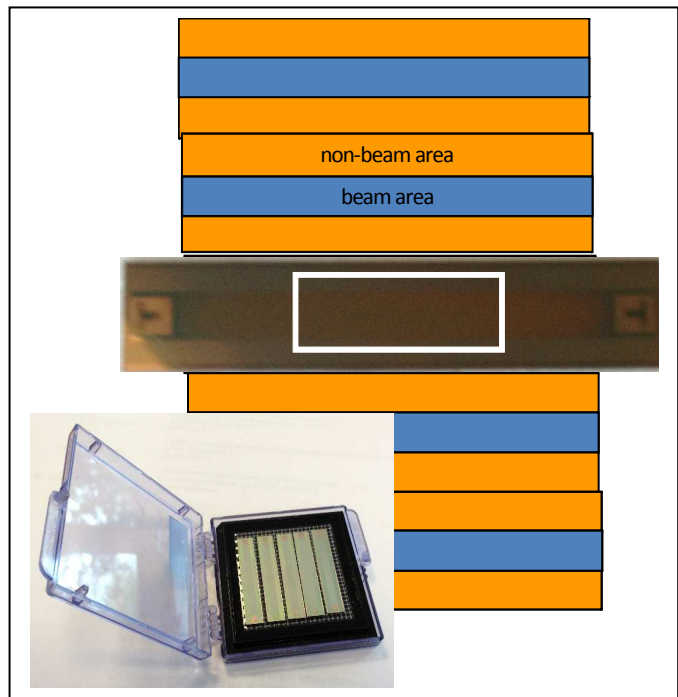


Figure 2. Lay-out of the blanker plane, showing the non-beam areas which are used for connections and water cooling. The white box on the blanker chip indicates the area used for the 1wph tool.

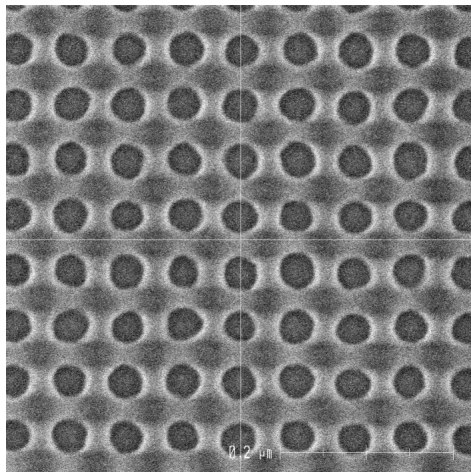


Figure 3. 32 nm hp dense contacts written with the Asterix prototype at $42 \mu\text{C}/\text{cm}^2$. 3 sigma value is 3.5 nm.

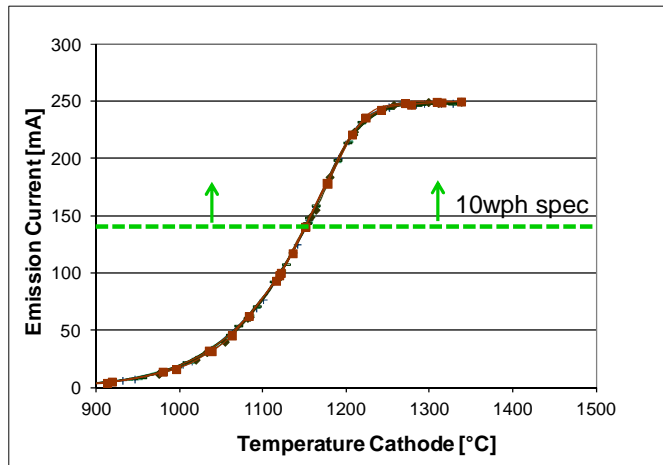


Figure 4. Emission current of the source for the MATRIX system.