## Defect Management of EUV Masks: Progress and Outlook

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This presentation aims to provide an overview of progress and challenges in the handling of defects on masks for extreme ultraviolet (EUV) lithography. Major tasks in mask defect management include mask inspection, repair, cleaning, transportation, and storage. For EUV masks, inspection must be performed on mask blanks and patterned masks. For inspecting blank defects buried in or underneath the multi-layer (ML), the effectiveness of the 193nm-wavelength-based system is examined via a mask blank with programmed defects. Initial results obtained from an actinic inspector will also be reported. In the inspection of patterned masks, absorber film stack needs to be tuned to optimize the contrast of captured images. To gain resolution, the performance of an e-beam inspector is evaluated and compared with that of the optical tool.

Mask repair in EUV lithography consists of the usual repair of defects present in the absorber material and compensation for the effect of the ML defects. Precise control of the height and sidewall angel is required in absorber repair. For ML defects, repair of bumps and pits on the low thermal expansion material (LTEM) substrate prior to ML deposition is studied to improve blank quality. Compensation repair in the absorber is experimented, with the attempt to recover to some extent the lost lithographic process window due to the ML defects.

Mask cleaning in EUV lithography consists of front and backside particle removal. New chemical implementation with recipe optimization is employed to improve the particle removal efficiency (PRE) without absorber "shrinkage" and ML capping layer damage. Since the backside of the mask is pattern-free, physical force can be implemented in the cleaning to achieve high PRE.

Without suitable materials for a pellicle, fall-on defects tend to appear during mask transportation and exposure in the EUV scanner, prompting increased frequency of mask re-inspection. A no-pellicle mask handling flow is investigated to enable development and initial manufacturing of devices using EUV lithography.