Sub-10 nm silicon nano-structures based on block copolymer lithography and high selectivity, cryogenic temperature dry etching

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Patterning using block copolymer directed self-assembly is a powerful technique for high density nanomanufacturing, for example in semiconductor patterning or bit patterned storage media. To capitalize on advances in BCP lithography, plasma pattern transfer must advance in parallel. We studied cryogenic plasma etching, first introduced by Tachi *et. al.*,[1] down to sub-10 nm scale towards production of densely packed silicon wires, holes and fins from various block copolymer derived masks and polymer resists. Etching anisotropy is created by forming a thin $SiOF_x$ sidewall layer at cryogenic temperatures in a SF_6/O_2 plasma.[2] Upon returning to room temperature the passivant becomes a thin SiO_2 layer.[3] For example, using PS-PDMS block copolymer lithography, sub-10 nm silicon wires were produced (Figure 1). TEM images reveal ~ 8 nm crystalline silicon wires surrounded by a thin amorphous oxide layer (Figure 1 inset).

With careful micron and deep nanoscale etching we show that cryogenic temperature etching can provide extreme selectivity and anisotropy at the nanoscale even with soft masks. Selectivity is enhanced while maintaining pattern verticality because resist etch rates decrease as temperature is lowered (Figure 2). Resist etch rate studies in different diluted oxygen chemistries show that the resist etch rate is significantly reduced in the presence of SF_6. Resist etching rate is suppressed with etching time and corresponds to fluorination of the resist. Using the SF_6/O_2 process, Si pattern transfer is achieved with no intermediate hard mask and very thin PS masks (13 and 6 nm) created from BCP lithography using PS-*b*-P2VP (Figure 3). Higher selectivity can be achieved with a chromium hard mask as used in Figure 1. Aspect ratios of greater than 12:1 were achieved and limited by silicon wire collapse during etching. Temperature control was also important in the chromium etching to prevent migration of the PDMS spheres created after etching the PS from a PS-PDMS BCP pattern. Simulation work shows the role of oxygen and ion angular distribution in the silicon profile evolution.

References:

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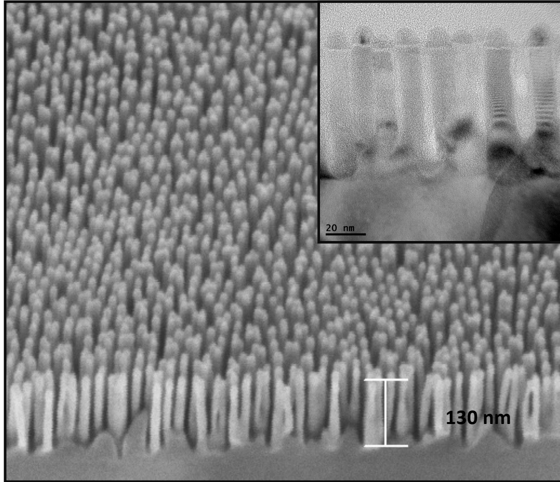

Figure 1: Silicon nanowire forest created with PS-*b*-PDMS BCP lithography and cryogenic silicon etching. Inset is TEM images of the nanowires. Moire fringes on right indicate a crystalline core surrounded by a thin amorphous layer.

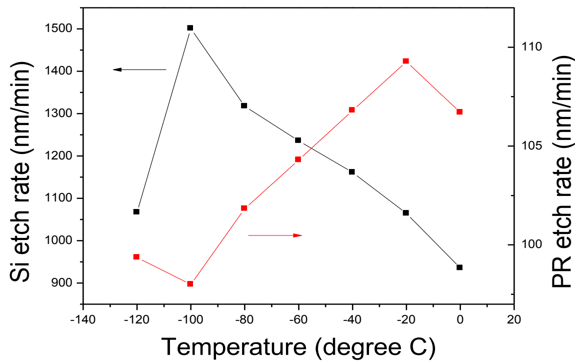

Figure 2: Graph of silicon etch rate (feature depth of 1.5 micron features) and photoresist etch rate at constant oxygen flow and RF power. Photoresist etch rate decreases with temperature. The silicon etch rate increase with temperature is an artifact of a non vertical profile due to overpassivation at this oxygen level.

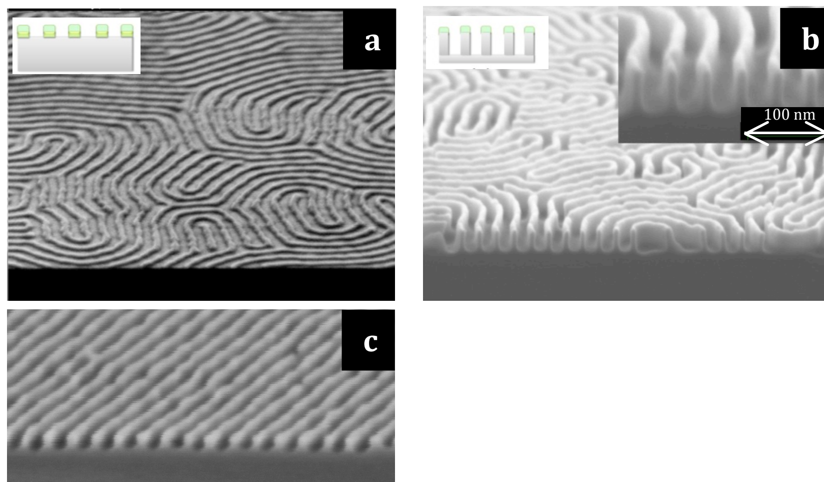

Figure 3. Silicon etched using only a PS hard mask derived from PS-*b*-P2VP. a) 13 nm thick PS lines at 21 nm half-pitch. b) Silicon etched using soft mask from a). c) Silicon etched from 6 nm thick mask at 13 nm half-pitch.