Prototype Active-Matrix Nanocrystalline Silicon Electron Emitter Array for Massively Parallel Direct-Write Electron Beam Lithography

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This paper presents our latest achievements on the prototype active-matrix electron emitter array for high-speed massively parallel direct-write electron-beam (e-beam) lithography. The whole system embodies an array of microcolumns, each having an electron emitter array integrated with a MEMS condenser lens array in combination with microminiaturized electron optical elements for projecting a reduced image (1/100) of focused e-beams (see Fig.1).[1] The electron source is a nanocrystalline Si (nc-Si) ballistic emitter in which a 1:1 projection of the e-beam can resolve patterns 30 nm wide.[2] A structure of arrayed dot patterns of the nc-Si emitter is integrated with an active-matrix driving LSI.

The device structure is schematically illustrated in Fig.2 (a). The electron-emitting part of the device consists of an array of nc-Si dots fabricated on a Si substrate and via-first-processed Through Silicon Via (TSV) plugs of poly-Si connected to the dots from the back of the substrate. The device consists of an aligned joint of poly-Si plugs with driving pads on the active-matrix LSI. Figure 2 (b) shows a corresponding photographic image of the electron emitter array integrated with a 1st-prototype active-matrix LSI[1], having a 100×100 bit cell array with a 100-µm pixel pitch. The unit was designed to be able to simultaneously drive all the pixels of the nc-Si electron emitter array in accordance with a bitmap image preliminarily stored in a built-in memory. Next design of the LSI is currently under prototyping, in which each of the driving voltages in the picture cells can be controlled so that the aberration can be compensated on the projected image. Figure 3 shows cross sectional SEM images of the fabricated structure array, consisting of a 200×200 dots pattern of nc-Si emitters with a 50-µm pixel pitch. The pitch of the backside poly-Si electrode was adjusted during the patterning process to the same pixel pitch of the driving LSI, i.e., 100µm, so as to properly form an aligned joint with each other. Each of the columnar poly-Si top surfaces could be selectively anodized with a Si_3N_4 mask in a HF solution by galvanostatically applying an anodic current via the TSV plugs from the back of the substrate. This process successfully promoted preferential local dissolution at the poly-Si grain boundaries and resulted in structured nc-Si. Electron emissions from this structure array worked as intended (see Fig.4), indicating that the designed function of switching on and off the beamlets is properly performed by changing the CMOS-compatible voltage.

References

[1] N. Ikegami et al.: J. Micro/Nanolith. MEMS MOEMS **11**(3), 031406 (Jul–Sep 2012) (2012).
[2] A. Kojima et al.: J. Vac. Sci. Technol. **B** 26(6), 2064 (2008).

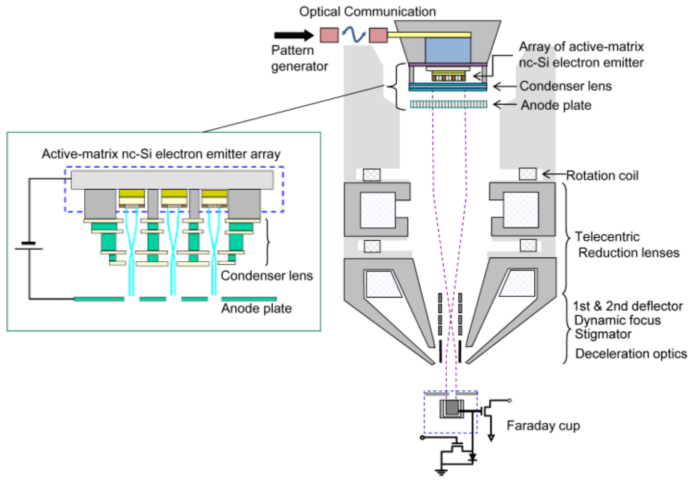
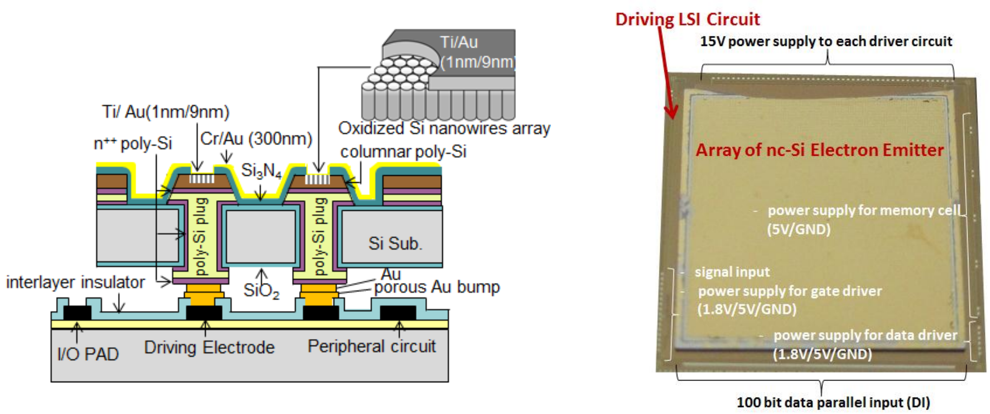


Fig.1: Configuration of the miniaturized column having an active-matrix nc-Si electron emitter array in combination with microminiaturized electron optical elements.



(a) (b)

Fig.2: (a) Schematic illustration of the structure of active-matrix nc-Si electron emitter array integrated with a driving LSI, (b) corresponding photographic image of the prototype.

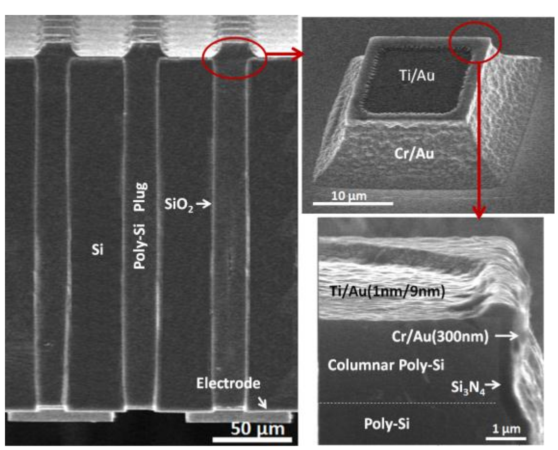


Fig.3: Cross sectional SEM images of the array of nc-Si electron emitter.

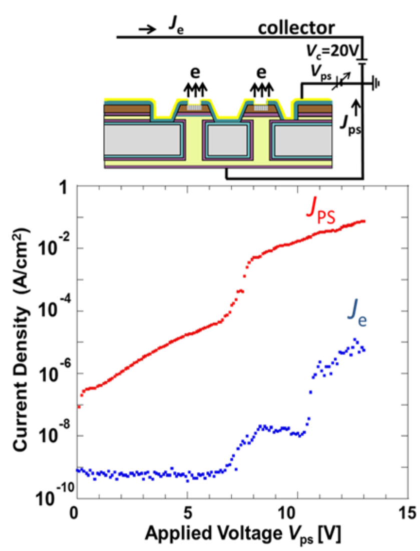


Fig.4: Characteristics of diode current density J_{PS} and corresponding emission current density J_e vs. applied voltage V_{PS}.