

Low line edge roughness patterning with Character Projection EB Lithography for Photonic Devices

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Photonic devices have relatively large pattern width compared with leading edge Si LSI circuit. For example the width of Si wire waveguide core is about 500nm for $\lambda = 1.55\mu\text{m}$. But it needs extremely small line edge roughness (LER) to realize low-loss waveguides. LER should be less than a couple of nanometers. Therefore when variable shaped beam (VSB) type electron beam (EB) writer, which is more than ten times faster in throughput than point-beam EB, is used for photonic devices especially with curvilinear patterns, sophisticated data preparation techniques are adopted to reduce step-like roughness¹⁻².

Character Projection (CP) type EB writer we've been developing has several advantages compared with VSB. (1) Shot count reduction and high reproducibility with application specific CP (ASCP) shots, (2) uniform pattern edge profile because only CP stencil defines the profile³. (3) Shape correction on substrate by using specialized software⁴.

In this paper we introduce a comprehensive CP data processing system for low LER patterning with CP EB writer whose data architecture is shown in Figure 2. In Figure 3(a) four triangles in dotted line is exposed by single shot of the ASCP. If ASCP is not prepared, whole rims of patterns are exposed by standard CPs like horizontal/vertical rectangles, octagon and so forth. And inner areas of patterns are exposed by VSB. Low LER can be observed in SEM photographs.

And some optical parameters of photonic devices fabricated by this method will be reported.

References

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- 3) M. Kurokawa et.al., Proc. SPIE 8081, 80810A (2011)
- 4) M. Takizawa et.al., Proc. SPIE 8522, Photomask Technology 2012, 85222A(December 6, 2012)

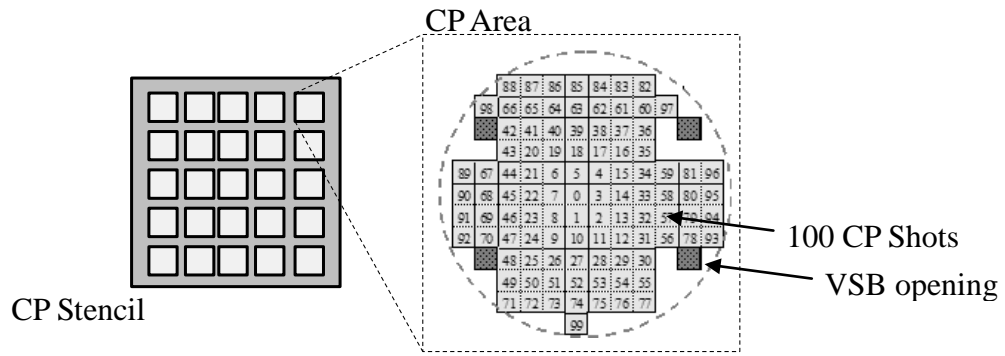


Figure 1: The schematic diagram of CP Stencil

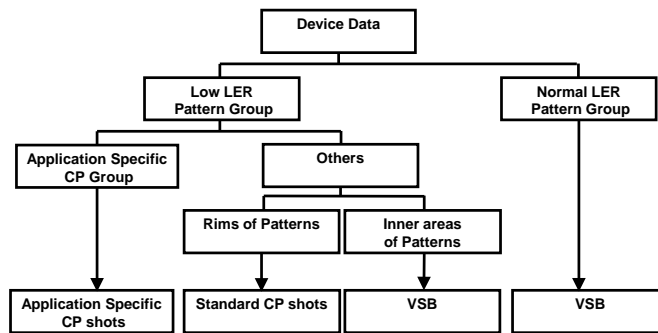


Figure 2: The architecture of EB exposure data for low LER patterning with CP EB writer.

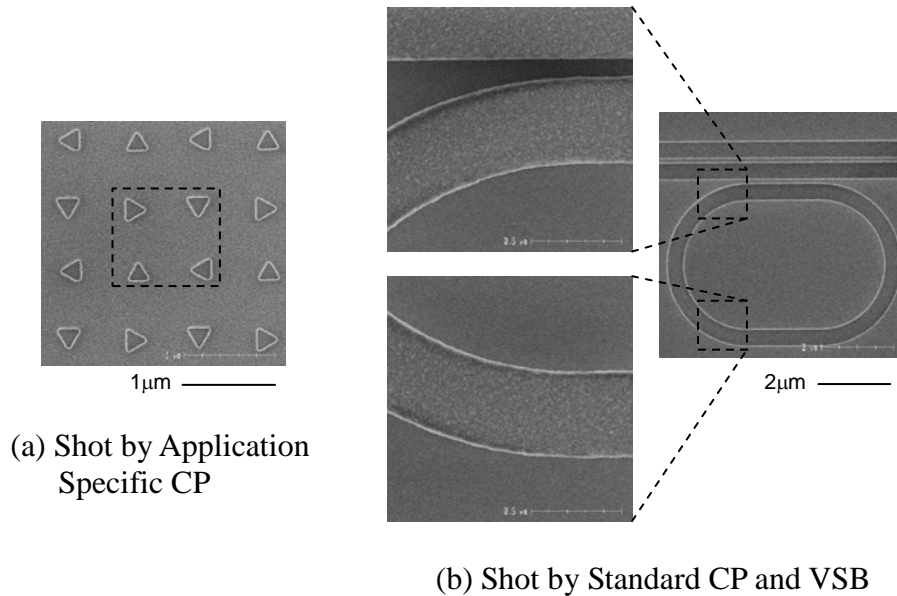


Figure 3: The SEM photographs of the exposed patterns by using CP technologies: (a) Four triangles in dotted line is exposed by single shot of the application specific CP. (b) Whole rims of patterns are exposed by standard CPs and inner areas of patterns are exposed by VSB.