# Fabrication of p-type Silicon Nanowires for 3D FETs Using Focused Ion Beam

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Focused Ion Beam (FIB) system have been used for sub-32 nm and 3D devices, such as FinFETs and Si nanowire ([1, 2]). FIB system allows Si substrate milling to achieve dimensions smaller than sub-10 nm of nanochannel diameter ([2]). Furthermore, FIB system provides the depositions of Pt, Au, W electrodes and SiO2 dielectric. In this context, in this work, FEI Nova 200 NanoLab FIB system (Figure 1) was used for local Gallium doping and Silicon nanowire (SiNW) fabrication on SOI wafer for 3D FETs.

First of all, SOI wafers were cleaned with a standard RCA method. Then, a conventional furnace with $O_2$ + $H_2O$ ambient at 1000 ºC for 180 minutes was used to oxidize the silicon layer (340 nm) on buried oxide (400 nm) of SOI wafers. Thus, a thinner silicon layer of 15 nm was obtained (Figure 1(a)) after the BHF wet etching of silicon oxide grown on SOI wafer. Optical lithography and RIE plasma were carried out to define the Si active region, where it will be fabricated the 3D devices (Figure 1(b)). To get a p+ type SiNW, $Ga^+$ local implantation (beam energy of 10 keV and dose of $1x10^{14}$ $cm^{-2}$) on active region using FIB was used. Rapid Thermal Annealing (RTA) was carried out at 1000 °C during 60 seconds in nitrogen environment for Ga dopant activation. Figures 1(c) and 1(d) present the p+ Si NW definition on SOI substrates using $Ga^+$ FIB (energy of 30 keV and ion current of 50 pA) thinning of active region width of 45 µm to 35 nm, resulting in a Si NW with these dimensions: width of 35 nm, length of 6 µm and thickness of 15 nm. EDS measurements of p+ Si NW were carried out before and after RTA process and are shown in Figure 1 (h). Before RTA, Si, O and Ga elements on SiNW were detected, due to the Si milling using $Ga^+$ ion beam to define the SiNW and local implantation to get p+ region. After RTA, however, no signal of Ga element was detected, only Si and O elements, which confirms that Ga dopant has become electrically active in crystalline net of silicon. It is important to notice that O element detection is from the BOX of SOI wafer. After RTA, Pt deposition using FIB was carried out to form the source/drain electrodes, which is also shown in Figure 3. Thus, using the back side of wafer as back gate electrode, we have a pseudo MOS (Figures 1(f) and 1(g)) ([3]). Figure 2 presents drain-source current ($I_{DS}$) versus drain-source voltage ($V_{DS}$), for different values of back gate voltage ($V_{GS}$), and also presents $I_{DS}$ versus $V_{GS}$, for different values of $V_{DS}$. Both curves show very similar behavior to the SiNW transistors that was presented in reference 2, indicating that our process for device prototype fabrication based on Ga local implantation, Si NW definition and Pt deposition using FIB can be used to get 3D transistors, such as FinFETs and junctionless.

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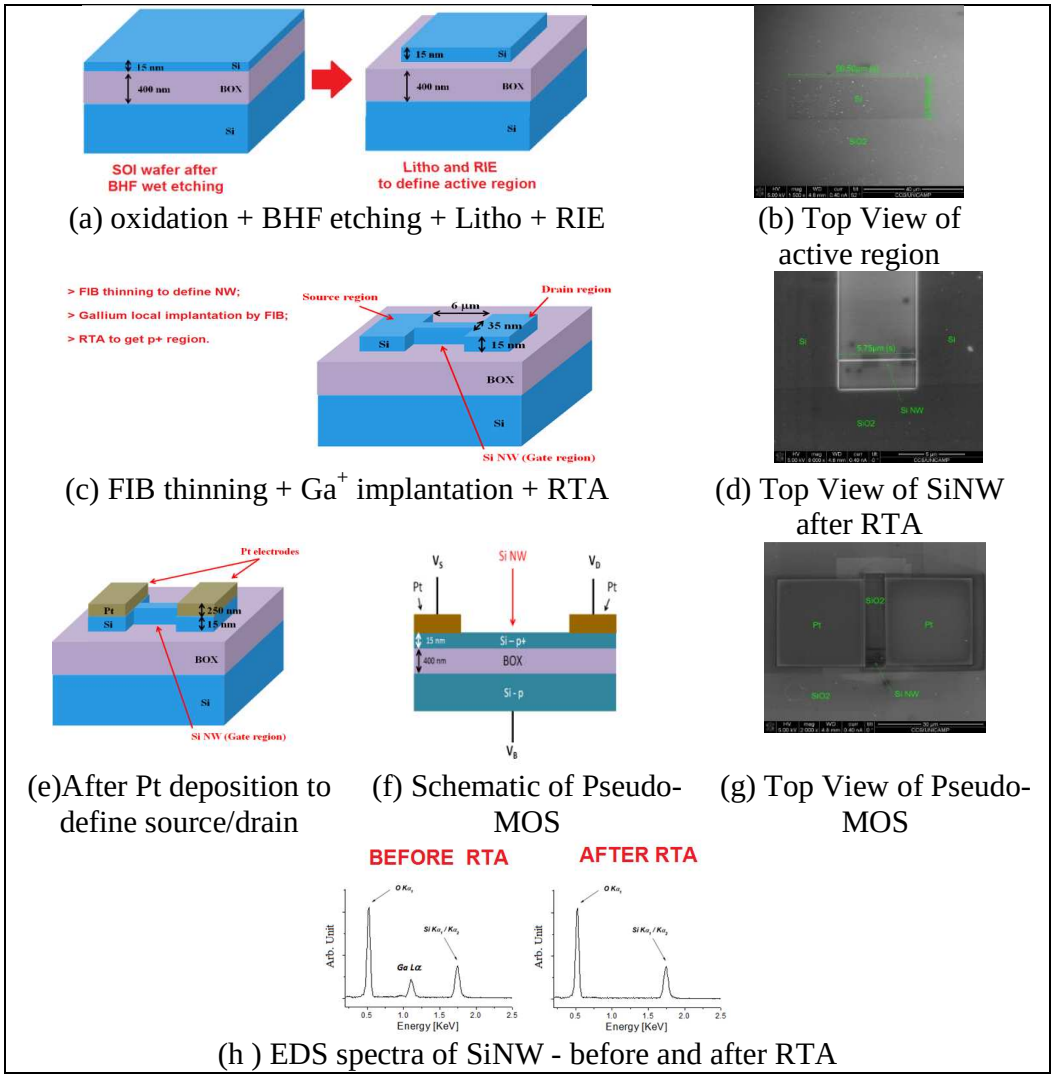


(a) oxidation + BHF etching + Litho + RIE

(b) Top View of active region

(c) FIB thinning + $Ga^+$ implantation + RTA

(d) Top View of SiNW after RTA

(e)After Pt deposition to define source/drain

(f) Schematic of Pseudo-MOS

(g) Top View of Pseudo-MOS

(h ) EDS spectra of SiNW - before and after RTA

*Figure 1:* Between (a) and (g): Process steps of pseudo MOS fabrication; and in (h): EDS spectra of SiNW.

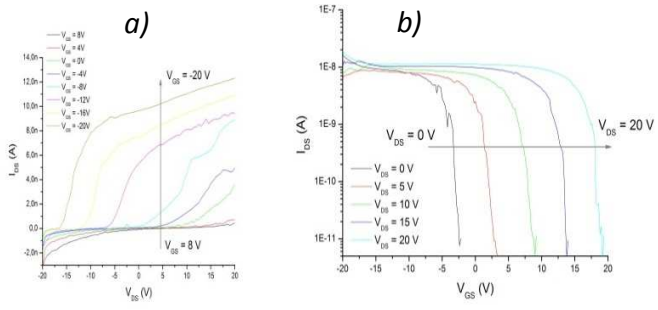


*Figure 2: a)* $I_{DS}$ x $V_{DS}$ and *b)* and $I_{DS}$ x $V_{GS}$ curves for Pseudo-MOS.