Crossbar Arrays of Sub-10 nm Memristive Devices Fabricated with Nanoimprint Lithography

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Memristors or memristive devices are two terminal bipolar resistive switches that are promising for the next generation non-volatile random access memory (NV-RAM) and beyond[1, 2]. Nanoimprint lithography (NIL)[3] has been demonstrated as an effective patterning approach for crossbar arrays of sub-25 nm memristive devices[4].

Here we present crossbar arrays of memristive devices with sub-10 nm feature sizes fabricated by using NIL. The molds of 8 nm feature were shrunk using 1:50 diluted hydrofluoric (HF) acid from a SiO_2/Si (100 nm thermal SiO_2 on Si) master mold with arrays of 50 nm wide wire arrays, nano- and microscale fanouts and 50 μm contact pads. The sub-10 nm SiO_2/Si molds were then duplicated into quartz (QZ) slides using NIL and dry etching to achieve vertical sidewalls hence better critical dimension (CD) control.

We used the QZ daughter molds to pattern both the top and bottom electrodes of the device arrays. First, thin layers of PMMA and UV-curable resists were spin coated on a Si wafer with 100 nm thermal oxide. After NIL, a two-step reactive ion etching (RIE) process was conducted to remove the residual UV resist and the PMMA layer. Next, a 10 nm thick Pt bottom electrode (with a 3 nm Ti adhesion layer) was deposited in an electron beam evaporator and lifted off in acetone. A 6 nm thick titanium oxide film was deposited by Ti evaporation and oxidization. Lastly, the top electrodes were defined in an NIL step with nanowires aligned orthogonally to the bottom ones, followed by RIE, evaporation (12 nm Pt) and liftoff.

Fig. 1 shows an SEM image of part of the fabricated device array. After electroforming, the devices exhibited non-volatile bipolar resistive switching behavior. The programming current of the 8 nm devices was about 600 pA, much lower than those for larger devices (Fig. 2). In addition to ultralow power consumption, the 8 nm device also demonstrated fast switching speed and improved performance repeatability.

Furthermore, imprint molds with sub-6 nm feature sizes were also successfully fabricated using electron beam writing and wet etching (Fig. 3). The 6 nm device fabrication and electrical characterization will be presented.

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1 Chua, L. O. *IEEE Trans. Circuit Theory* **18,** 507-519 (1971).
2 Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. *Nature* **453**, 80-83 (2008).
3 Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Science* **272**, 85-87 (1996).
4 Qiangfei Xia, EIPBN2011.

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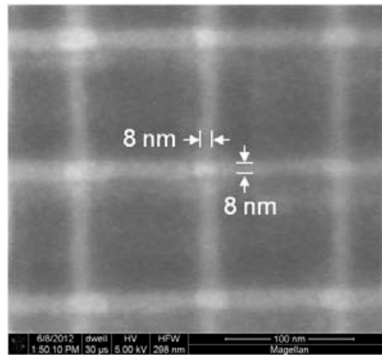

Figure 1: SEM image of an 8 nm cross-point memristive device array.

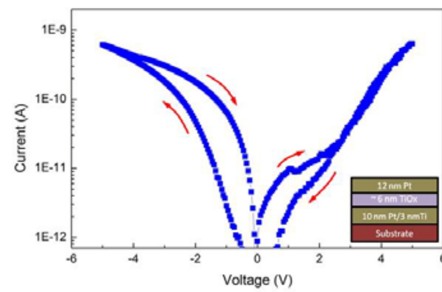

Figure 2: Typical switching behavior of an 8 nm device with sub-nA programming current. The cross sectional device geometry is schematically shown in the inset.

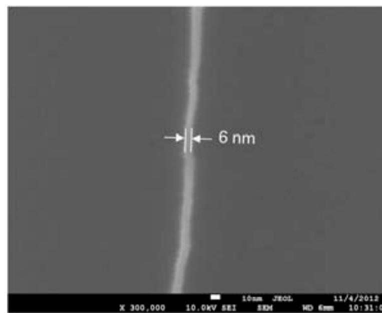

Figure 3: SEM image of a 6 nm wide silicon wire on an imprint mold.