Line width roughness reduction strategies for resist patterns printed via electron beam lithography

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Keywords: electron beam lithography, resist line width roughness (LWR), post-litho processes, roughness spectral analysis (PSD)

Preferred presentation mode: ORAL PRESENTATION

ABSTRACT

With the constant down-scaling of features in the semiconductor industry, Line Width Roughness (LWR) is considered as the factor limiting the miniaturization. In recent years, several papers showed the importance of post-lithography processes to reduce LWR and reach the ITRS specifications[a]. In this study several techniques to decrease the LWR of Line & Space patterns printed via electron beam lithography are investigated. The following techniques are discussed and compared: thermal treatments, plasma treatments, in-track surfactant rinse and use of under-layers. All the exposures of this study are made with a Vistec shaped-beam tool SB3054DW with an acceleration voltage of 50kV. The resist used in this study is the current champion positive CAR resist designed for 5kV multi-beam lithography and qualified in the CEA-LETI environment on the Mapper equipment. The final objective is to transfer the LWR reduction protocol developed on 50kV exposures to 5kV multi-beam exposures. All the LWR measurements are made with a Hitachi CDSEM HCG4000. Frequency analysis of LWR is carried out and a PSD (power spectrum density) fitting method is used to obtain an unbiased value of LWR[b] as well as spectral information on the LWR. The techniques exhibit a reduction of the LWR in the medium and high frequency domain. So far the most promising result is a decrease in LWR of 20%. The aim of the study is to assess to what extent LWR can be mitigated with all the treatments combined and study the LWR during metal gate stack patterning.

[a] www.itrs.net
[b] L. Azarnouche et al. J. Appl. Phys. 111, 084318. (2012).

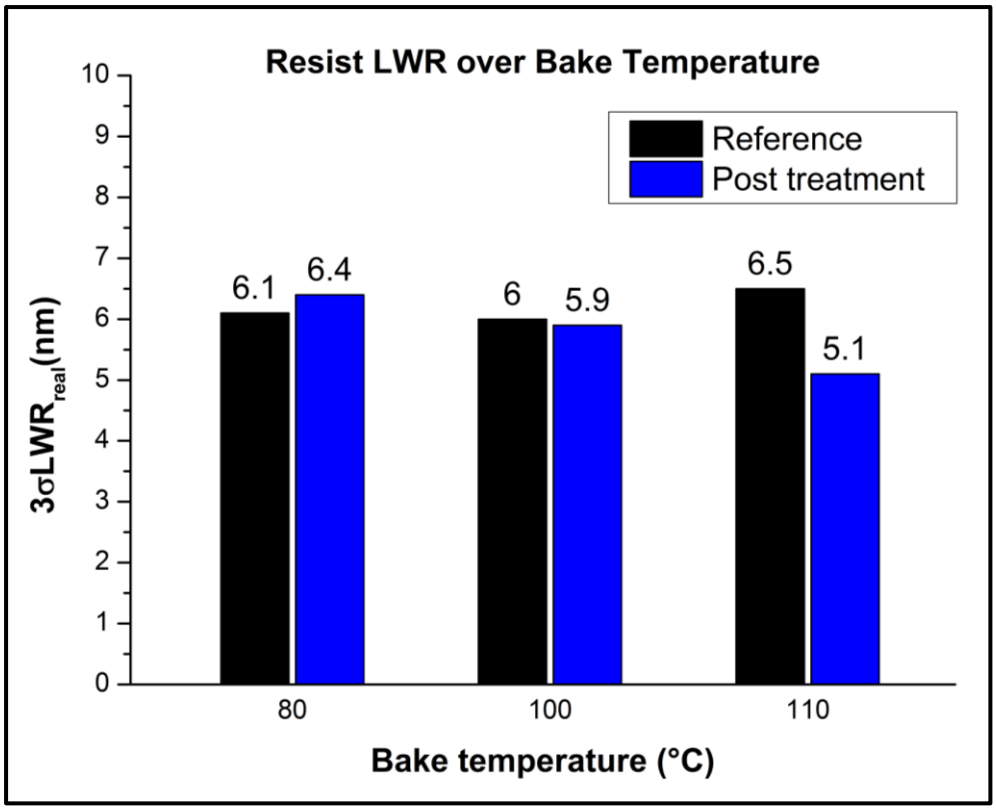

Fig.1: Impact of thermal treatment on resist LWR as a function of bake temperature. Each bake lasts 5 minutes.

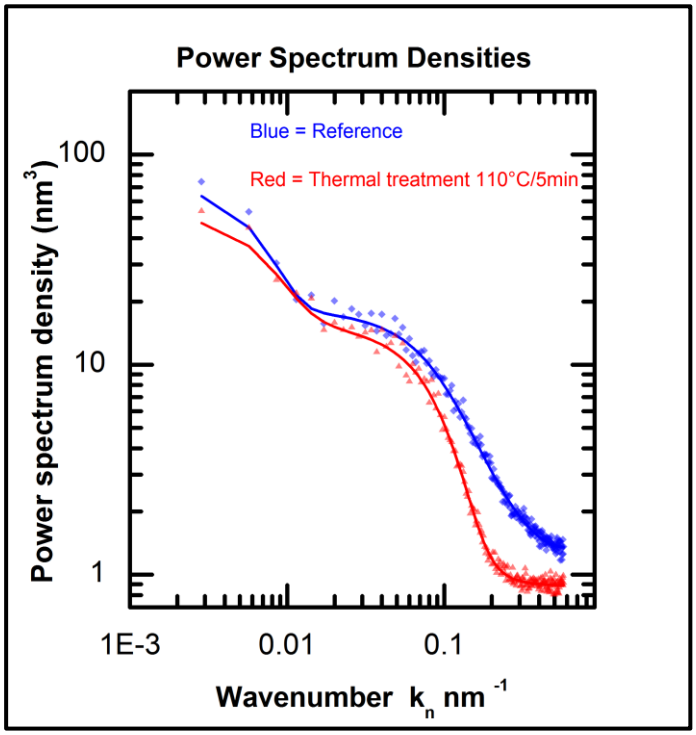

Fig.2: Power spectrum densities of LWR before and after a bake of 110°C over 5 minutes. Triangles and squares represent experimental data. Straight lines represent the PSDs of the fits.