# Inductively Coupled Plasma Etching of Through-Cell Vias in Indium-Bearing III-V Solar Cells Using $SiCl_4$/Ar plasma

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Dry etching of indium-bearing III-V heterostructures is an important process technology in RF and optical applications, typically with a need to achieve smooth and vertical etch profiles [1,2]. While etches for III-V In-based heterostructures with good morphology have been demonstrated[1,5], emerging applications require wafer-scale, dense via arrays in more complex and thicker III-V heterostructures, posing a considerable challenge. Here, a novel wafer-scale etch process for fabricating dense arrays of small-area through-cell vias for advanced InGaP/GaAs/InGaAs inverted metamorphic (IMM) triple junction photovoltaic cells is reported. A diagram of the heterostructure used is shown in Fig. 1; the epitaxial layers are 14 μm thick in total.

Inductively coupled plasma reactive ion etching (ICP-RIE) of III-V semiconductors in $Cl_2$-based plasma has been widely discussed [3-5]. However, due to the varying compositions in heterostructure devices, achieving the required sidewall profile can require multi-step etches[3], increasing process complexity and reducing throughput. A promising alternative to $Cl_2$-based etching is $SiCl_4$; this etchant has been reported to produce a more favorable etch profile due to the mass effect from $SiCl_x^+$ species in the plasma[6]. In this work, via-etch processes based on $SiCl_4$/Ar gas mixtures were explored for through-cell etching; the etch conditions were optimized to obtain smooth and vertical etch profiles, using an Oerlikon Shuttleline ICP-RIE system with He backside cooling. Both small samples as well as full 100 mm wafers were evaluated to assess etch rate and profile uniformity and loading effects.

Etch parameters evaluated include pressure, $SiCl_4$/Ar flow rate ratios, and RIE powers: the key trends are highlighted in Fig. 2. As can be seen, a selectivity higher than 14 was obtained under all conditions evaluated, which was sufficient for the through-cell etching with the 1.25 μm thick $SiO_2$ mask used. Etch rates greater than 600 nm/minute were achieved, leading to reasonable processing times. Pressure had a strong influence on etch rate and selectivity (Fig. 2). However, as shown in Fig. 3(a-b), higher pressure also results in undercut in the In-containing quaternary layers. Likewise, reducing RIE power also increases the undercut in quaternary and and InGaAs layers (see Fig. 3 (c-d)). Fig. 3(e) shows the etch profile for a typical 30 μm via etched on a full 4" wafer under the optimal etch conditions: 5 sccm $SiCl_4$, 10 sccm Ar, 100 W RIE/300 W ICP power, 0.6 mTorr, and 180 $^0$C. Good sidewall morphology is obtained with etch rate variation of less than 3% across a 4" wafer. Optical emission spectroscopy was used to monitor the etch (Fig. 4(a)) and loading and aspect ratio effects[7] have been evaluated (Fig. 4(b)).

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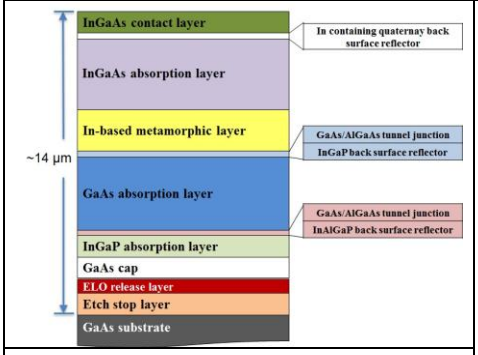


*Figure 1: Schematic diagram of the heterostructure. The overall epitaxial layer thickness for etching is approximately 14 μm.*

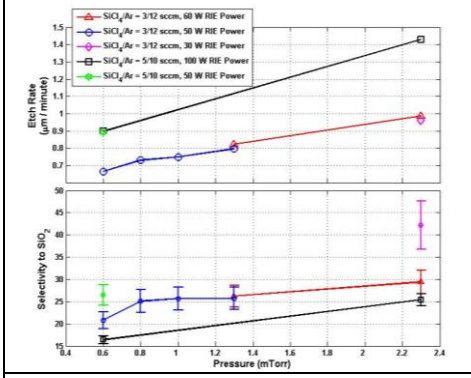


*Figure 2: Etch rate and selectivity to $SiO_2$ of different etch conditions. (All other process parameters held constant: 300 W ICP Power and 180 °C.)*

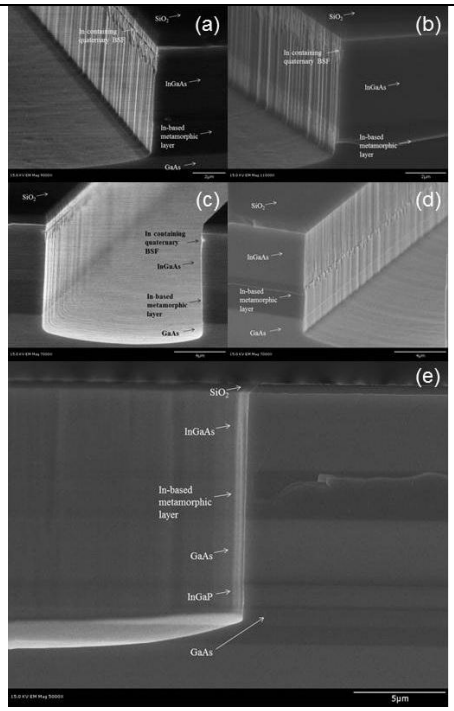


*Figure 3: SEM micrographs of the triple-junction solar cell heterostructure etched with (a) 1.0 mTorr, and (b) 0.6 mTorr; (c) 50 W, and (d) 100 W RIE power. The other process parameters of (a) and (b): 3 sccm $SiCl_4$, 12 sccm Ar, 50 W RIE power, and of (c) and (d): 5 sccm $SiCl_4$, 10 sccm Ar, 0.6 mTorr. (300 W ICP power and 180 ° C held constant). (d) SEM micrographs of the 4'' triple-junction solar cell wafer etched under the optimal etch conditions.*

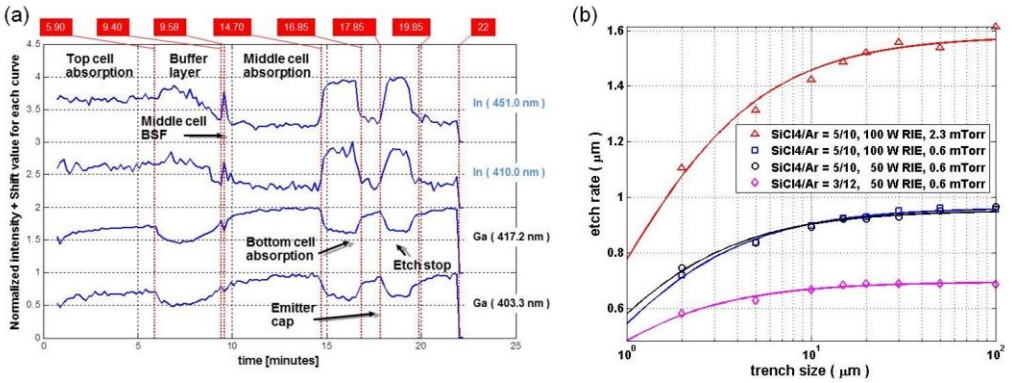


*Figure 4: (a) An OES time-scan for the typical Indium and Gallium emission peaks. (b) Size effect on the semiconductor etch rate. The solid lines are the model calculation results and the markers show the experimental data.*