Patterning of Light-Extraction Nanostructures on Sapphire Substrates Using Nanoimprint, SiO_2 Masking and ICP Dry Etching

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A central challenge in light emitting diodes (LEDs), a key element in energy saving lighting, is light extraction. The un-extracted light not only wastes energy, but also heats up LEDs and greatly shortens lifetime, both substantially increasing lighting cost. The higher a material index, the more light will be trapped and the worse in light extraction (Hence GaN LEDs have the worst light extraction). Nanostructures patterned on sapphire substrates can greatly improve the light extraction in GaN LEDs, and can improve epitaxial crystal quality which increases the quantum efficiency[1]. Previously, nanopatterning in sapphire suffers the issue of shallow depth, because (a) in wet etching, it is limited by $(11\bar{2}2)$ plane[2] and (b) in dry etching it is limited by the mask used. Here we present a fabrication process that allows the nanopillars (200 nm pitch and sub-150 nm diameter) etched into sapphire with much deeper depth and steeper sidewall over the previous wet etching and dry etching. Furthermore, the process uses nanoimprint patterning, which is a natural choice for LED manufacturing.

Our process involves: nanoimprint, pattern transfer into SiO_2, and ICP dry etching with SiO_2 mask (Fig.1). Specifically, (1) A 350 nm-thick SiO_2 layer was deposited on sapphire by PECVD, followed by spin-coating of a sub-layer (NXR-3022, Nanonex) and a UV resist (NXR-2030, Nanonex); (2) UV nanoimprint on SiO_2 surface using a mold with 200 nm-pitch pillar and 125 nm pillar diameter; (3) a 10 nm-thick Cr was evaporated and lift-off; (4) the oxide layer was etched by fluorine-based RIE to transfer nanopattern and then Cr was removed; and (5) the sapphire substrate was etched by ICP (chlorine-based chemistry) with the oxide as the mask, creating nanopillars on sapphire substrate with sub-150 nm in diameter and > 140 nm in depth.

The SEM pictures show (a) UV nanoimprint transfers nanopatterns to resist with high fidelity (Fig. 2a); (b) a 3.5-minute ICP etching results in 145 nm etching depth, and a sidewall slope of 70°, indicating that the SiO_2 mask barely shrunk during ICP etching (Fig. 2b,c); and (c) however, if the SiO_2 mask is replaced by Cr mask, under the same etching condition, the final etched profiles will be poor: a much shallow etching depth (only 52 nm - 2.6 times less deep) and small sidewall slope (only 40° - far less vertical) (Fig. 2d). The far worse etching profile in Cr masking than SiO_2 masking is attributed to the facts that (i) the chlorine-based ICP chemistry attacks Cr more than SiO_2, causing serious mask edge erosion and (ii) the by-product from Cr etching greatly reduce the sapphire etching rate (possibly by re-deposition).

In summary, our work develops a dry etching method using nanoimprint, SiO_2 masking, and ICP etching for sapphire nanopatterning to achieve deep etching depth, sharp sidewall and easy lift-off process. The process developed here can be scaled to large volume manufacturing.

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[1] H. Chen, C. Wang, and S. Chou, EIPBN 2011.

[2] K. Kim, *Trans. Electr. Electron. Mater.* 2009 (10), 40.

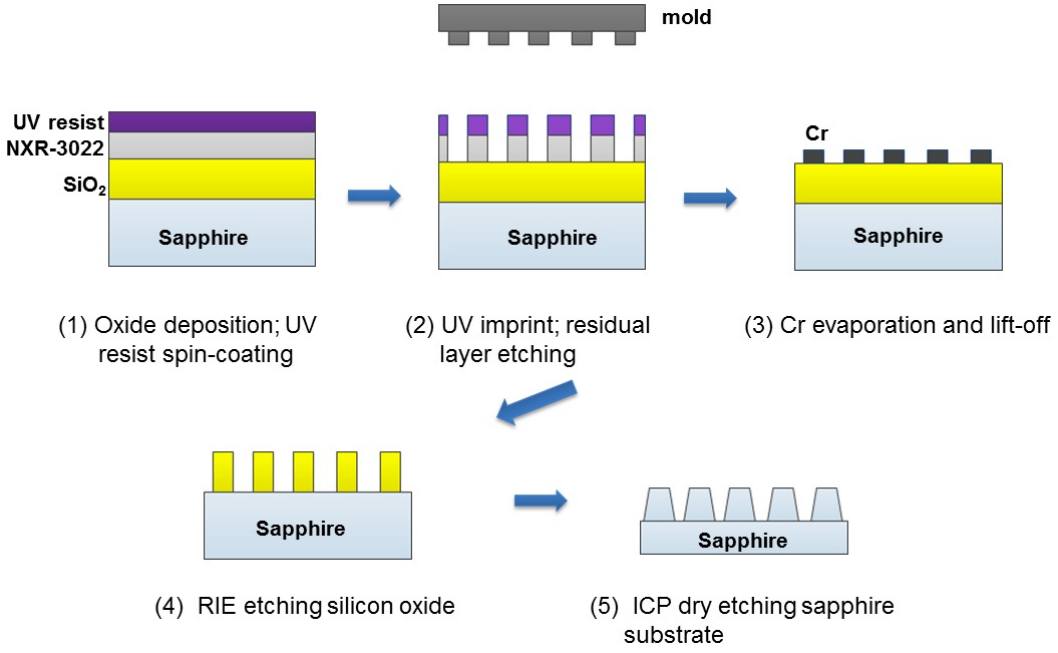

Fig. 1. Nanopatterning sapphire substrate process: nanoimprint lithography, Cr lift-off, SiO_2 nanostructure mask etching, and ICP dry etching of sapphire substrate.

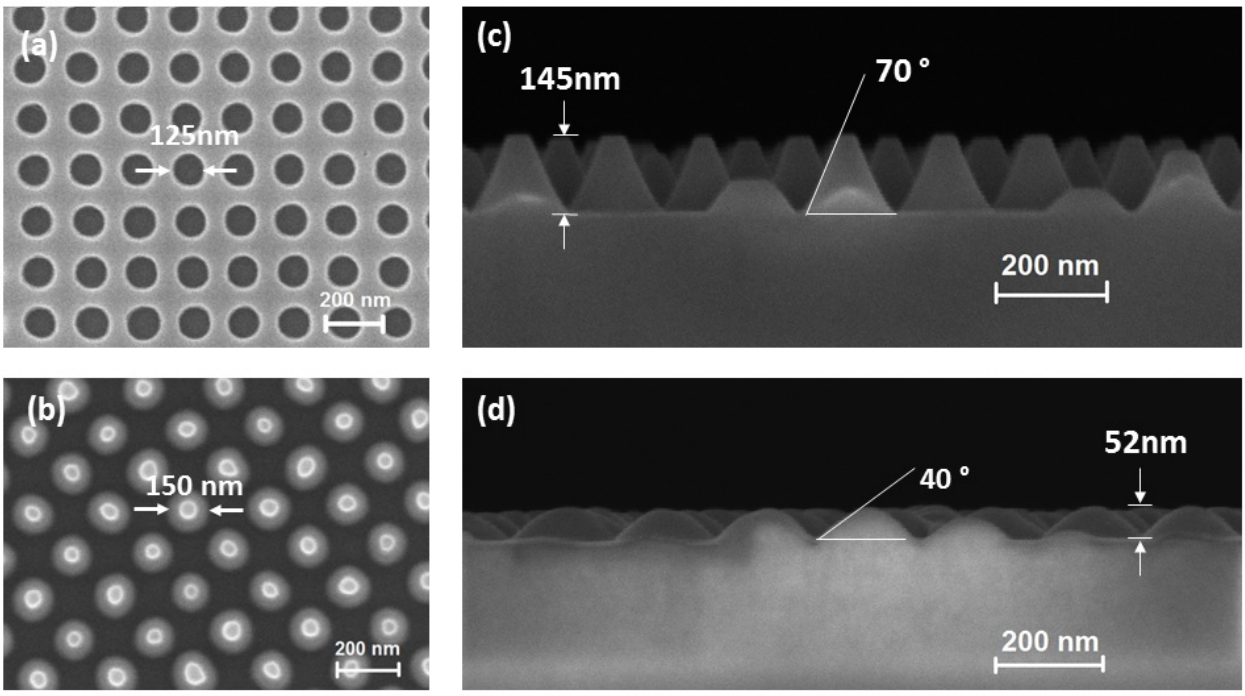

Fig. 2. (a) Sub-wavelength pattern on UV resist after imprint; (b) top view of etched sapphire substrate by ICP using SiO_2 mask; (c) profile of etched sapphire pattern masked by SiO_2 layer, showing 145 nm depth and sidewall slope of 70°; (d) the same ICP etching but with 40 nm Cr replacing SiO_2 mask, leading to a much shallow etching depth (only 52 nm - 2.6 times less deep) and small sidewall slope (only 40° - far less vertical).