High Resolution Patterning with Electron-Beam Lithography and Sidewall Image Transfer

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Pattern definition at or below 30nm feature pitch is challenging for any direct lithography technique, including electron-beam lithography (EBL). Successful EBL exposures down to 10nm pitch have been reported[2] using conventional EBL systems and high contrast resist processes. At such small feature sizes, however, system noise issues can become a limiter of resolution, density, pattern placement, and/or edge roughness, especially when large patterns are exposed and exact tolerances are required[3]. For these reasons, it becomes interesting to explore sublithographic resolution enhancements as a way to extend the resolution of EBL without requiring aggressive tool or resist process optimization.

Sublithographic patterning using sidewall image transfer (SIT) or self-aligned double-patterning (SADP) has become common practice in advanced CMOS manufacturing[4]. Reports of EBL combined with SIT have also been published, demonstrating resolution down to 36nm pitch[5]. In this work, we explore process issues associated with pushing this technique to the 20nm pitch regime. We also present a method for arbitrary unidirectional pattern generation using this technique.

The basic steps of the SIT process are illustrated schematically in Fig. 1. In our process flow, EBL accomplishes the base lithography (down to 40nm pitch) using Hydrogen Silsesquioxane (HSQ) resist and conventional 0.26*N* TMAH development. The HSQ pattern is transferred into an underlying carbon layer using reactive ion etching (RIE) in a reducing chemistry. In this work we explored both CVD deposited amorphous carbon and a naphthalene-based spin-on carbon for use as a sacrificial mandrel material. Two different conformal films were investigated for the sidewall spacer: HfO_2 and TaN. In both cases the film was deposited by atomic layer deposition (ALD). In practice, TaN permitted the use of a slightly thinner SIT spacer (down to 4nm) than HfO_2 (down to 6nm). Using either material, we achieved 20nm pitch line/space patterns. Figure 2 shows SEM images of line/space patterns at different pitches after pattern transfer into the silicon substrate. As shown, our SIT process is relatively insensitive to the mandrel thickness.

The SIT process is excellent at creating a grating-like pattern. The creation of arbitrary unidirectional patterns is possible using additional lithography and etching or deposition processes. In this work we demonstrate this by fabricating the gate level of a CMOS logic block with 30nm pitch features. Additional EBL and RIE processes were inserted after SIT spacer formation and before final pattern transfer. SEM micrographs shown in Fig. 3 depict the entire process step by step. Accurate customization of the SIT grating pattern is limited by overlay. In our case, the overlay was tightly controlled and allowed defect free pattern generation as shown in Fig. 3g-h. We will discuss further details of the process integration and pattern transfer process in addition to the pattern decomposition method required to generate the mandrel and customization pattern data from conventional layouts.

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[2] J. K. W. Yang et al, *J. Vac. Sci. Technol.* B **27**, 2622 (2009).

[3] E. Kratschmer et al, *J. Vac. Sci. Technol.* B **31**, 06F405 (2013).

[4] C. Auth, *VLSI Technology* 131-132 (2012).

[5] J. Belledent et al, *Proc. SPIE* **8323**, 83230F (2012).

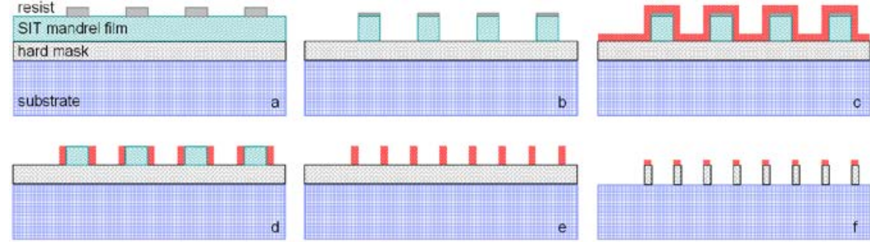

Figure 1. Schematic cross section cartoons of the SIT process flow, doubling the pitch of a line/space pattern. (a) mandrel definition by the base lithography, (b) mandrel etch, (c) conformal film ("spacer") deposition over the mandrel shapes, (d) anisotropic spacer etch, (e) mandrel removal, and (f) pattern transfer into the hard mask or target film stack. The SIT spacer can subsequently be removed.

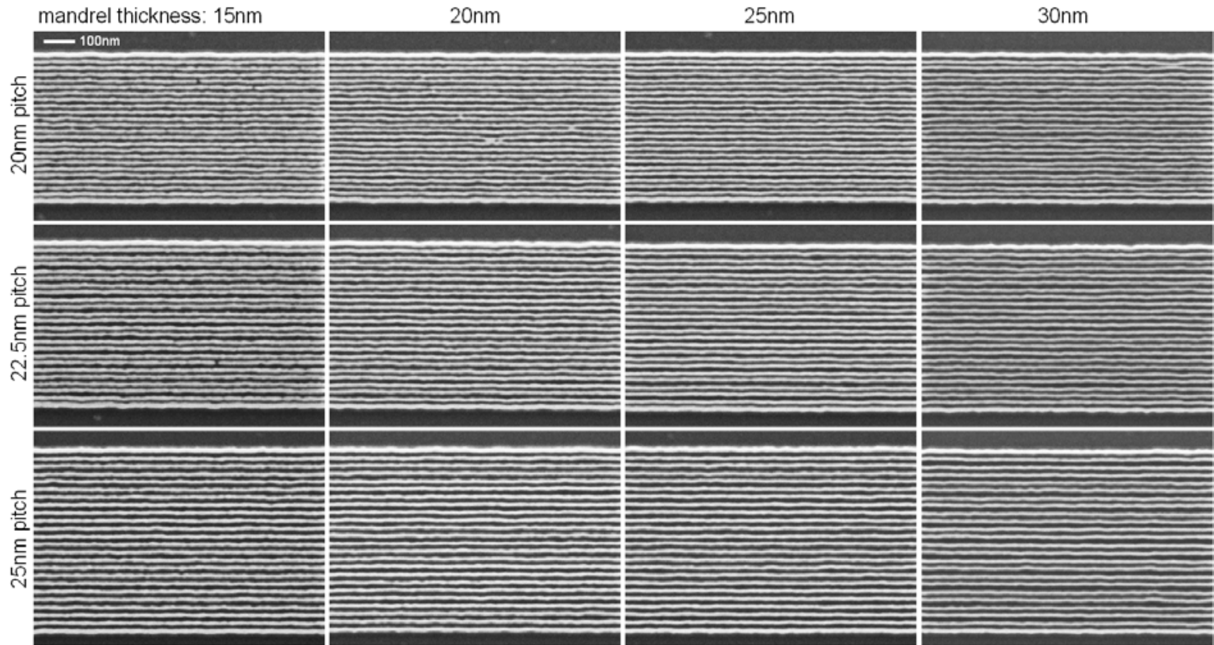

Figure 2. Process window of our EBL + SIT flow with HfO_2 spacer. SEM images are taken at the end of the above SIT flow (Fig. 1), after pattern transfer into the silicon substrate. They show line/space patterns at 20nm, 22.5nm, and 25nm pitch across 4 different mandrel thicknesses. All SEM images are taken at the same magnification and working distance and have an identical scale bar, shown at the top left.

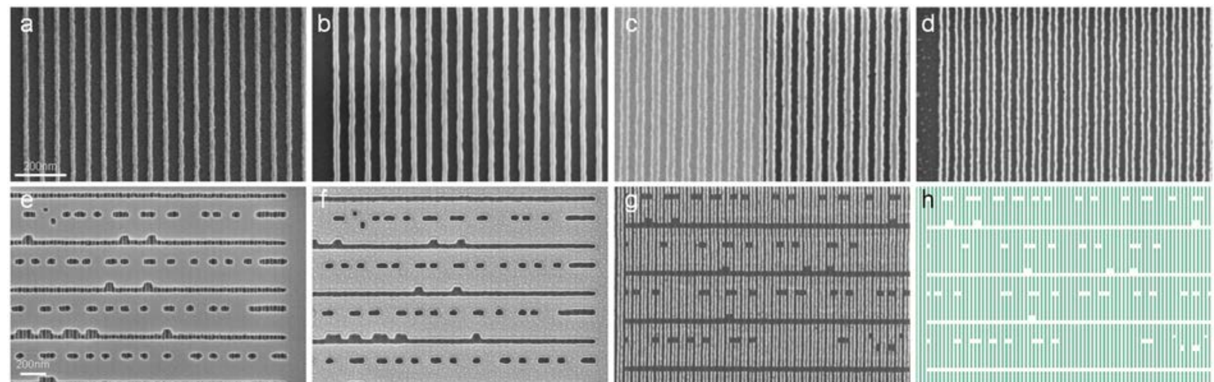

Figure 3. SIT flow with cut mask process for pattern customization, resulting in a unidirectional CMOS gate pattern at 30nm pitch with no defects and flawless pattern fidelity. The top row of images follows the standard SIT flow: (a) base lithography, (b) mandrel etch, (c) spacer deposition and anisotropic etch [right half shows secondary electron image, left half is a backscatter image], (d) mandrel removal. The bottom row illustrates the grating customization (at lower magnification): (e) aligned cut mask exposure, develop, and transfer, (f) etched SIT spacer to customize grating, (g) cut mask removal and pattern transfer. The last figure (h) depicts the target pattern clip corresponding to location (g) on the hardware, demonstrating excellent pattern fidelity.