

# Cross point Si/SiO<sub>x</sub>/Si resistance switches fabricated by stacking single-crystalline fluid-supported Si membranes

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Resistive random access memory (RRAM) is believed to be a promising candidate for next generation memory due to its scalability to sub-10 nm, fast switching speed, long retention time and high endurance.<sup>1</sup> In recent years, silicon and silicon oxide based RRAM devices have drawn increasing interest because of the materials and processing compatibility with current integrated circuit (IC) industry.<sup>2</sup> In this abstract, we report the fabrication and characterization of crossbar RRAM devices based on chemically produced silicon oxide<sup>3</sup> with single-crystalline silicon electrodes fabricated by stacking fluid-supported membranes. The devices showed bipolar resistive switching behavior with high ON/OFF ratio and good cycle-to-cycle uniformity.

Commercial Soitec smart cut silicon-on-insulator (SOI) wafers (70 nm thick device layer, 140 nm thick buried oxide) were used for both bottom and top electrodes. The device layer was heavily doped with spin-on glass ( $5 \times 10^{20}$  borosilica film from Emulstone) followed by thermal diffusion at 950°C for 30 min. The bottom electrodes were fabricated on one SOI wafer by photolithography and reactive ion etching (RIE) (Figure 1). Wet chemical process using Piranha solution (H<sub>2</sub>SO<sub>4</sub> and H<sub>2</sub>O<sub>2</sub> with 3 to 1 volume ratio) was used to produce 1-nm thick silicon oxide on the surface of bottom electrodes as the switching layer.

To fabricate the Si top electrodes, the heavily doped device layer on another SOI wafer was released and transferred to the first SOI wafer as a fluid-supported membrane.<sup>4</sup> To facilitate the membrane release, nanoimprint and RIE were firstly employed on the SOI wafer to create uniform nano-holes arrays of 200 nm pitch. The RIE selectivity between nanoimprint resist and silicon was increased by a 45-degree tilt evaporation of 10 nm Cr. After liftoff, the wafer was immersed into 10:1 buffered oxide etcher (BOE) to release the silicon device layer, which was then floated in deionized (DI) water in another beaker. The SOI wafer with bottom electrodes was used to pick up the floating Si membrane, followed by baking at 95°C and annealing at 500°C on a hotplate. Figure 2 shows the 0.5 cm wide holey Si membrane before and after being transferred to the wafer with bottom electrodes. Finally, photolithography and RIE were employed to pattern the Si membrane into top electrodes. Figure 3 shows optical and scanning electron microscope (SEM) images for the fabricated 4×4 crossbar devices array. The top and bottom electrodes are both 3 μm in width and 500 μm in length.

Before electrical measurement, a short HF dip was used to remove the native oxide to expose Si on the contact pads. The devices exhibited repeatable bipolar resistive switching behavior. Figure 4a,b show typical IV curves for the fabricated devices. The turn on voltage ( $V_{SET}$ ) is -6 V and turn off voltage ( $V_{RESET}$ ) is 7 V. It is noteworthy that the operation voltages were read from two wire measurement, and the electrode wire resistance was high (about 20 kΩ), so the actual voltages across the junction were much lower. The device also exhibited a high ON/OFF ratio of  $2 \times 10^3$  at -0.5 V. The OFF state conductance was rectifying while the ON state was Ohmic, with a resistance about the same as that of an electrode wire. Figure 4c plots the 50 consecutive cycles of switching, demonstrating good cycle-to-cycle uniformity.

<sup>1</sup> J. J. Yang, D. B. Strukov, and D. R. Stewart, *Nat. Nanotechnol.* **8**, 13 (2013)

<sup>2</sup> J. Yao, Z. Sun, L. Zhong, D. Natelson, and J. M. Tour, *Nano Lett.* **10**, 4105 (2010)

<sup>3</sup> C. Li, J. Hao, and Q. Xia, *Appl. Phys. Lett.* **103**, 062104 (2013)

<sup>4</sup> S. Ghadarghadr, C. P. Fucetola, L. L. Cheong, E. E. Moon, and H. I. Smith, *J. Vac. Sci. Technol.* **B 29**, 06F401 (2011)

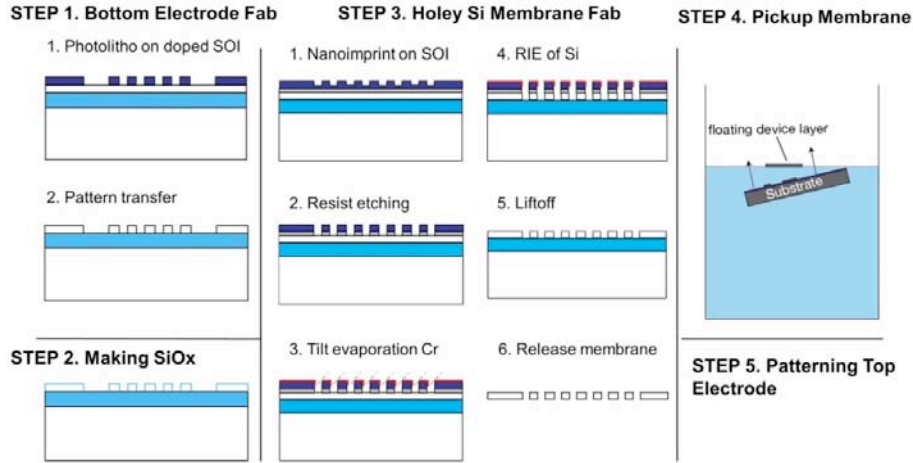


Figure 1: Schematics for fabrication processes. STEP 1 and STEP 2 are on one SOI wafers fabricating bottom electrodes, STEP 3 are on another SOI wafer fabricating releasable membrane.

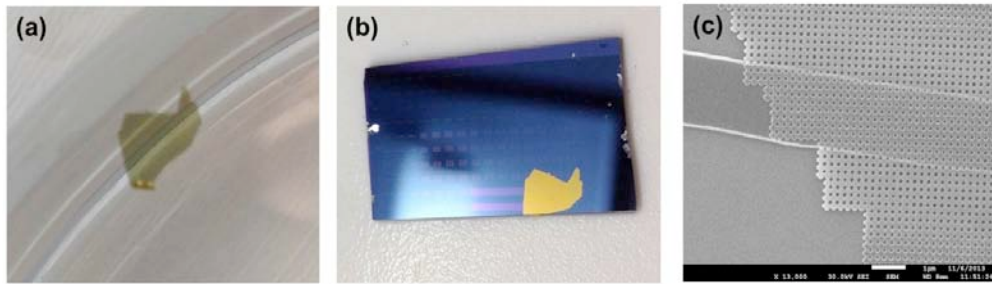


Figure 2: (a) Picture for fluid supported single-crystalline silicon membrane, which is about 0.5 cm large; (b) Picture for another SOI wafer with patterned bottom electrodes and transferred membrane stacked on top; (c) SEM picture for part of the membrane with holes array.

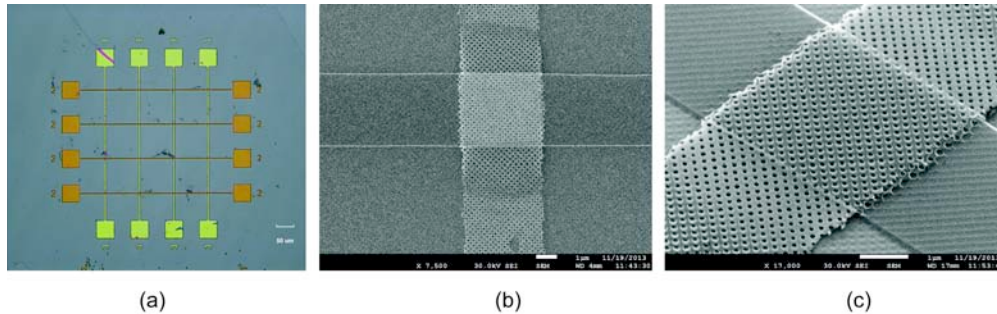


Figure 3: (a) Optical image for  $3\mu\text{m}\times 3\mu\text{m}$  crossbar devices; (b) top view SEM image for one cross point device, and (c) bird-eye view SEM images for the device in (b) with a higher magnification.

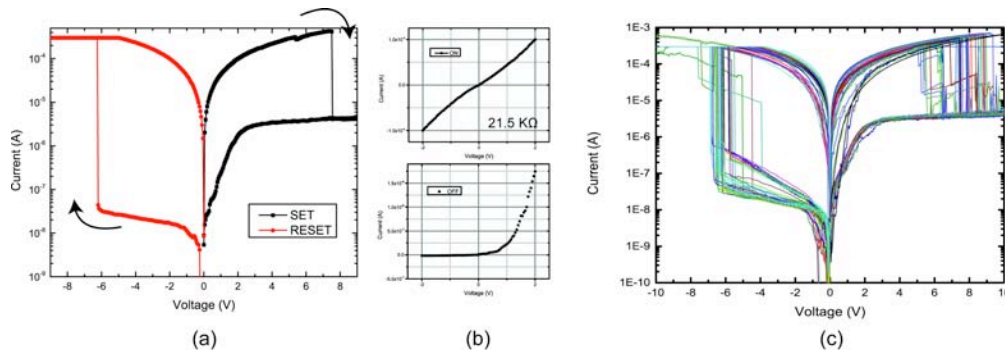


Figure 4: (a) Typical switching curve for the crossbar device; (b) The ON state is Ohmic with resistance about 21.5 k $\Omega$ , and OFF state shows obvious rectifying behavior. (c) The 50 cycles switches shows good cycle-to-cycle uniformity.